Analog signal capabilities – 729Analyzer - V7.0 Grant Saviers 12/30/05

GOALS AND DESIGN PHILOSOPHY:

1. Minimum state in the analog section.
2. All clocking provided by the Up controller in the digital section.
3. IRG delays, access times to first data bit, etc. all established by uP.
4. Record lengths are established by uP. There are no record length counters in the analog section.
5. Read after write delay of the read signal is established by the uP.
6. Simulate as much real world tape and drive characteristics as practical.
7. Provide adequate read signal channel amplitude and timing variations to fully exercise the TAU.
8. Permit the emulator to be daisy chained with other tape drives.
9. Enable more features if uP performance or memory are increased.

CAPABILITIES

Simulate 729 II/V and 729 IV 200 & 556 bpi and 729 V 800 bpi read signals (5 pulse frequencies). Only the high density analog pulse width is provided, for 41.67, 62.5 & 59.96 kHz (II/V and IV 556bpi and V 800bpi respectively). 200bpi signals may be adequately reproduced to be properly detected, tbd by testing.

DATA FORMAT

6 bits of data are provided and 1 parity bit is computed, converted to NRZI polarity information and loaded by the uP, for each bit period into the POLARITY register via control signals SELRCDR and ANALOGSTRB. This permits the uP to force VRC errors at any point in the data block. LRC is provided by the uP as the last character and thus LRC errors can be forced.

Read after write signals can be generated by the uP by delaying the simulated write data bits the time appropriate for the speed of the tape and the write to read head gap dimension.

The analog signal outputs are enabled as long as the SELECT line is enabled. Any spurious transitions of the PULSE or POLARITY registers when SELECT is not enabled may cause noise on the output lines to the TAU.

SIGNAL CONVENTIONS IN THIS DOCUMENT

uP bus signals and the A through D multiplier value registers are referred to as byte quantities, numbered 0 to 7, LSB to MSB.

The PULSE and STROBE registers that generate analog signals are referred to by their 729 tape channel names, 1,2,4,8,A,B,C LSB TO MSB (8^{th} bit not used for tape signal control, but may be used for other purposes.)

LOGIC FAMILY

The 74HCxyz family is used because of good noise immunity, equal pull up and pull down impedances, equivalent (and more) functions to 74S/LS series, widely available at low cost including on ebay, and I had a bunch on hand.

REGISTERS

Six 8 bit registers are located on the analog board:

PULSE for controlling the timing of the output NRZI analog "1" signal, bits <0:6> correspond to tape drive read tracks <1:C>.
POLARITY for controlling the polarity of the output NRZI analog pulse, bits <0,6> correspond to tracks <1:C>, NRZI recording requiring alternating polarities for sequential "1" values, except for simulated error conditions.
RCAA – RCAD (Read Channel Amplitude A-D), four registers to control the amplitude of the NRZI output signal, with 7 4 bit hex digits as the multiply value of n/15 times the output voltage. The msb 4 bits of RCAD are not used.

These registers D inputs are buffered by a 74HC541 octal non-inverting 3 state buffer which has inputs connected to microcontroller PORT D <0:7>.

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READ SIGNAL AMPLITUDES

Each channel amplitude is controlled by 4 bits of a register (RCAA through RCAD). The 4 high order bits of a 10 bit multiplying D/A converter, ADI 7533, control the signal amplitudes provided for each channel. The remaining 6 multiplier bits are tied to a ground. A hex 0 outputs no analog signal (multiplier is zero) and a hex F outputs the maximum peak to peak amplitude of 10 volts. This value is 2 volts higher than the specified setpoint of the 729 read preamplifier using an IBM voltage calibration tape. The register assignments are as follows:

Register bits	Function	Control signal (ANALOGSTRB)
RCAA <0:3>	Channel 1 amplitude	SELRCAA
RCAA <4:7>	Channel 2 amplitude	SELRCAA
RCAB <0:3>	Channel 4 amplitude	SELRCAB
RCAB <4:7>	Channel 8 amplitude	SELRCAB
RCAC <0:3>	Channel A amplitude	SELRCAC
RCAC <4:7>	Channel B amplitude	SELRCAC

RCAD <0:3>	Channel C amplitude	SELRCAD
RCAD<4:7>	not used	

Registers are selected by a ground true signal (SELRCAA-D, SELRCDR, & SELRCPR). Data is loaded on the positive going edge of ANALOGSTRB. Setup times must be observed for the 74HC377.

ANALOG PULSE SHAPING

Preliminary NRZI "1" pulse shaping is performed by an RC circuit and final pulse shaping is an LC circuit. Actual analog pulse timing is derived from a register PULSE bits <1:C> which is turned on and off by the uP via SELRCPR and ANALOGSTRB. The leading edge of the simulated read analog pulse (positive or negative on the analog output bus) occurs on the register bit going to ground and held ground for a on time of approximately 8 to 9 usec. Positive and negative pulse peaks are slightly delayed from the end of the logic pulse. This enables skew and pulse crowding to be simulated independently on each channel if the uP can generate register changes quickly enough.

REPRODUCTION OF TAPE ANALOG READ SIGNALS

Given a control uP which can change the state of POLARITY and PULSE at a fast enough rate under program control, or by computing in advance an entire data block of register values at a clock rate several times the normal [tape density times tape speed] frequency and "DMAing" these values from memory to the registers at that high clock rate, the following signal conditions can be generated by the analog board:

1. Variable static gain per channel: Each channel can independently have its output voltage set to any of 16 levels between 0.0v and 10v peak to peak. Tape read signal amplitudes vary for a number of reasons, including gap width, throat height, tape magnetic parameters, tape velocity, 729 preamp gain settings, etc. IBM provides several checks in both the read and read after write conditions for read amplitudes. This capability permits testing of these various read and read after write circuits in the TAU. For normal operation, the read signal should be set to 8v p-p or hex C in the high and low order hex positions of the RCAA through RCAC registers, and low order position of the RCAD register.
2. LRC and VRC forced errors can be created by not simulating a "1" in the appropriate channel at the appropriate time and by correspondingly not toggling the POLARITY value for that channel for the next "1" that is simulated.
3. Drop-out simulation: Drop-outs are momentary decreases in the channel amplitudes, caused by a variety of sources which include dirt on the tape, defects in the magnetic coating, momentary head to tape separation, and others. They are easily seen in NRZI all "1's" data patterns. The ADI 7533 has a multiply output settling time of 600nsec so it is possible to change signal amplitudes on each channel dynamically for as many or few bits periods as desired at any shape of amplitude modulation between 10v and 0v p-p output.

4. Drop in simulation: (this should work, but haven't tried it) Drop-ins are easily seen in NRZI all "0's" data patterns. They are shorter the normal bit period and are bipolar pulses. The causes include holes in the magnetized tape magnetic coating, head to media capacitive discharges and impulse noise. They can be simulated by changes in the POLARITY register of the pattern

	1usec/bit	2usec/bit
POLARITY	00010000	0100
while PULSE is	00011000	0110

5. Pulse crowding: Clocking information is recovered from the data in the TAU by utilizing even parity and the requirement that 2 "1's"be written for the 1401 character BLANK. The TAU inserts these bits on channels C & A on a write and strips these bits on a read. Odd parity operations are also permitted which always have at least one "1" per bit period. The clock is recovered by a peak detection circuit for each channel and this clock is logically combined in the TAU to test the thresholded amplitude value of the read signal for each track. Signal peak positions are affected by recorded bit patterns. If the recorded sequence 00011000 is written and then read back in a channel, at a sufficient recording density, the peak of the first "1" will be early and the second "1" will be late. The density at which this occurs is affected by factors such as thickness and magnetic properties of the tape coating, head gap width, head to tape separation and others. The uP can simulate this situation by appropriate timing of PULSE register transitions.
6. Write and Read head skew: Provisions are made in the 729 drive via adjustable delay lines to independently align the timing of the 7 write and 7 read channels. Write skew is not meaningful since the TAU is writing to the uP memory during a write operation. However, in read after write operation, the read signal is delayed by the transport time of the tape moving the magnetic transition from the effective trailing edge of the write head gap to the center of the read head gap, plus signal delays in the analog signal chain. As the STROBE register allows independent control of each read channel's pulse position it is possible to simulate any combination of write plus read head skews. This feature may be useful in checking acceptable range of the derived combined clock of all channels in the TAU.
7. Other features, likely of dubious value: The circuits permit some things that are unlikely to occur in a magnetic recording channel.
    a. multiple sequential positive or negative read signal pulses can be created in any sequence.
    b. The circuits will also generate noise on the analog output bus to the TAU if the Analyzer is not SELECTed and the value of the PULSE and POLARITY registers are altered.
    c. Flat topped read pulses can be generated by PULSE values longer the approximately 12usec. Analog bus baseline voltage value will also shift

with even longer PULSE values. NRZI systems are also susceptible to generating low frequency signal components with extended runs of zeros between isolated ones.

CIRCUIT DESCRIPTION (see page 1 of schematics)

The uP data bus is buffered by a HC541 non-inverting octal buffer and then connected to all HC377 register's D inputs. Each register is selected by a separate uP generated select line which is at ground value to select the register and not buffered.

The selected register is loaded from the data bus on the positive transition of ANALOGSTRB, which is buffered by a non-inverting gate to create BANALOGSTRB and connected to the clock input of all registers. HC377 setup times must be observed by the uP.

The polarity of the read signal pulse is controlled by the POLARITY register. It is necessary for the uP to compute the NRZI signal polarities and provide the appropriate values to this register for each bit period. The HC377 octal D flip flop register tracks the value placed on the data bus when selected and clocked by ANALOGSTRB. *(We need to determine 729 read signal polarity conventions – is the first read signal pulse polarity sent to the TAU of a record from tape +, - or x?)*

The leading edge of each channel's simulated read signal pulse (i.e reading and NRZI "1" value) is established by the PULSE register appropriate bit transitioning to ground. POLARITY should be established at least 1 uP cycle prior to the PULSE transition, except for unusual operations such as drop-in generation. (generally, prop delays are insignificant relative to read channel bit periods). PULSE should be held at ground for 8 to 9 usec and then reset to high with a high level signal on the data bus by ANALOGSTRB and selecting the PULSE register. Note that the NRZI code requires a toggle of a channel bit in POLARITY preceding the corresponding channels PULSE transition.

The PULSE register bit for each channel is connected to the enable line of a 3 state HC125 buffer and the POLARITY register bit for each channel is connected to the HC125 buffer input. With the output off, the outputs are biased to 2.5volts by the 620 ohm voltage divider, which establishes the 3 state off state 2.5 volt value on the 0.01uf capacitor. When PULSE is low, the 3 state output turns on and the capacitor charges via the 332 ohm resister to +5 or ground, depending on POLARITY. When PULSE resets high, the capacitor is returned to +2.5 via a Thevenin equivalent 310 ohm source. This produces a basic pulse shape similar to that of a read channel, with reduced high frequency content.

See page two of schematics

The resulting basic pulse is connected to the Vref input of an ADI 7533 multiplier. This multiplier is set up for single quadrant operation, i.e. positive only input voltages and positive only multipliers. Only the 4 most significant bits of the 10 bit multiplier are used and are provided by the RCAA through RCAD registers. The lower order multiplier bits are set to zero via connection to ground, yielding a minimum multiplier of zero and a maximum multiplier of (512+256+128+64)/1023 or .938. Thus, the multiplier provides signal control from no output to maximum in 16 values, as follows:

value	HEX	voltage
15	F	9.99
14	E	9.33
13	D	8.66
12	C	8.00
11	B	7.33
10	A	6.66
9	9	6.00
8	8	5.33
7	7	4.66
6	6	4.00
5	5	3.33
4	4	2.67
3	3	2.00
2	2	1.33
1	1	0.67
0	0	0.00

The opamp LF353 is connected as required to the 7533. The 15pf negative feedback capacitor helps stabilize the opamp. The feedback to the 7533 is modified so allow gain in the LF353 stage by the resistor divider network 1.21k and 332 ohms. Due to the DC content of the signal the feedback is offset by 2 diode drops in order to not saturate the output of the LF353 to its positive or negative 12volt power supplies. Thus, a maximum peak to peak voltage of 10volts can be produced, in steps of 10/16 or .625 volts.

The DC component of the signal is removed by the .56uf coupling capacitor. The signal is further shaped by the low pass filter of 5mh and 470pf. These values are similar to those used in the TAU read amplifier input filtering. The resistor network of 8.66k and 7.87k establish a filter termination and bias point so that the output of the MPS404A silicon transistor emitter follower is slightly positive. The 63 ohm base resistor helps suppress oscillation of the emitter follower. The 1N4148 diode enables clamping the base to +6 volts which turns off the all emitter follower stages. Note that if the Analyzer is used concurrently with actual 729 drives, those drives can establish a –5 volt bus level, requiring a Vebo transistor rated at 15 volts or more, thus the MPS404A was selected.

The SELECT line is level shifted by a circuit of two transistors and 4 resistors, so that the unbuffered signal can hold all of the emitter follower bases to +6v via the 1N4148 diode network.

POWER ON STATE

The state of all registers is indeterminate at power on.

CONNECTORS see page three of schematics

The analog section is built as a daughter board and connects to the motherboard via a 60 pin flat cable. Pin assignments per page 3 of the analog circuit schematics. The board dimensions are 4.5 wide x 8.5 long and the connector is mounted mid-point on the long side adjacent to the motherboard. Logic ground should be star wired to the uP ground reference point and coax ground should be star wired to the commoned shields of the flat cable shields from the Analyzer to the shoe connector.

CONSTRUCTION

All IC's are DIP's and are inserted into wire wrap tail sockets. Discrete components, except for bypass capacitors are built on 16 pin DIP component carriers and inserted into sockets. The analog PCB is a .1" x .1" grid of plated through holes.

POWER SUPPLIES

Power voltages required are +5, +/-6, +/-12, all +/-2%. Current TBD. The power connector is located adjacent to the power supplies. Connector TBD. Electrolytic and ceramic bypass capacitors are liberally located on the analog board as near to semiconductor components as is practical.