D. M. GOLDSMITH.

IBM

Customer Engineering Manuals Supplement

System/Unit 7040-7044

Re: Form No. 223-2644

This Supplement No. S23-5013

Date December 9, 1963

Previous Supplement Nos. None

The information in this manual is a guide to the over-all picture of the 7040-7044, 1401 DPS operation, the control of data and instruction flow, and the over-all operation of the two systems when working as auxiliary units.

The instruction portion of this manual is a supplement to the Customer Engineering Manual of Instruction, 7040-7044 Data Processing System, Input-Output-Channel A Operations, Form R23-2652. The figures included in this manual are a supplement to the Customer Engineering Reference Manual, IBM 7040-7044 Data Processing System, Channel A, Form 223-2644. This arrangement of the material is not to be considered as an instruction-reference manual because this supplement was prepared with the sole purpose of supplying information on interface 5 until the revision of the above manuals is completed.

Since this material is supplementary, it is assumed that the reader is familiar with the information contained in the parent manuals; therefore, a detailed description has not been included on the operation of channel A.

International Business Machines Corp., Product Publications Dept., Poughkeepsie, N. Y.

PRINTED IN U.S.A.

FIGURE LIST

The IBM 1401 Data Processing System (DPS) is attached to channel A, interface 5, of the 7040-7044 DPS through the 1401 DPS Serial I-O Adapter (SF 7080). The 1401 Serial I-O Adapter allows a simplex mode of operation for transmission of commands and data between two data processing systems; that is, at any given time data transmission takes place either from the 7040-7044 DPS to the 1401 DPS, or from the 1401 DPS to the 7040-7044 DPS. The transmission of data between the systems is parallel by bit, serial by character. When the 1401 DPS is used as an auxiliary device on the 7040-7044 DPS, it is necessary to consider the I-O requirements, general specifications and description of the 1401 DPS Serial I-O Adapter, input-output signal and control lines, and the instructions used in both systems for control of data flow between the systems.

Input-Output Requirements

The basic requirements of various auxiliary devices are almost identical. For example, all auxiliary devices must be able to do one or more of the following: receive instructions to select the desired unit, write information on the unit, read information from the unit, start the desired unit, stop the desired unit, backspace a tape over one or more records, rewind a tape to its load point, select one of several stackers for the card just processed, and turn on indicators to indicate existing conditions (such as, unit is ready, unit requires attention, unit has stopped, a transmission error has occurred, or a special condition has occurred). Auxiliary devices also have in common such things as: data lines over which data are sent, data lines over which data are received, and a means of synchronizing the data flow between systems.

How these requirements can be met depends on the auxiliary unit. In a small, low-cost auxiliary unit, there usually is a limited amount of logical ability with a minimum amount of start and stop controls. Such a unit requires a number of individual control lines from the controlling system to tell it what to do; it also requires the system to supply data on the data transmission lines for an extended period of time if registers are not provided to contain the data. Usually units of this type are quite slow and the amount of data that can be transferred in any given time is relatively small. An example of such a unit would be the 1402 Card Punch attached to the 1414-4 I-O Synchronizer on the 7040-7044 Data Processing System.

In a larger more complex auxiliary unit (such as another computer), there is usually an extensive logical ability as well as complete start and stop controls. These units frequently require a minimum number of lines to and from the controlling system. An auxiliary computer can receive its instructions to perform various operations in the same way it received its data. The complex auxiliary unit can analyze the data; if the data were an instruction, it can perform the operation. In turn, the auxiliary unit can send status data back to the originating system over the data lines. The receiving system can analyze the status data to determine if the operation was successful or if transmission errors occurred.

In some cases, it is possible to connect the auxiliary unit to the controlling system by one cable. Such is the case when the 1401 Serial I-O Adapter is used to connect the 1401 DPS to the 7040-7044 DPS.

General Description and Specifications of the 1401 Adapter

The 1401 DPS Serial Input-Output Adapter has provisions for connecting one auxiliary unit to the 1401 DPS without requiring further modification of the 1401 DPS circuits; thus, the 1401 DPS is easily attached to the 7040-7044 DPS. The 7040-7044 DPS appears as an auxiliary unit to the 1401 DPS; of course, the 1401 DPS also appears as an auxiliary unit to the 7040-7044 DPS.

The following are recognized as standard considerations when the 7040-7044 DPS is attached to the 1401 DPS Serial Input-Output Adapter:

1. The attached 7040-7044 DPS must be interlocked with the 1401 DPS to permit two-way communication of signals.
2. Seven output data lines and seven input data lines transmit or receive one character at a time in parallel between the two data processing systems (serially by character). One character is made up of seven bits (six data bits and one parity or check bit).
3. Character transmission takes place at an 86 kc rate (11.5 microseconds per character).
4. The 1401 DPS clock is controlled by the 7040-7044 DPS after a read or write instruction has been transmitted to the 1401 DPS. The 1401 DPS does not perform other instructions between characters.
5. Data transfer proceeds between the 7040-7044, 1401 DPS when the RCHA instruction is executed by the 7040-7044 DPS and when the 1401 selects the I-O adapter with a read or write instruction. The data transfer will be terminated when the word count is reduced to zero in the 7040-7044 DPS or upon an end-of-record condition in the 1401 DPS. The 1401 DPS end-of-record condition occurs when a group-mark word-mark is encountered in the 1401 DPS core storage.

6. Each system must have a register for one character to be read into or out of during data transmission cycles. The 7040-7044 DPS uses the multiplier-quotient register for transmitting and receiving data; the 1401 DPS uses the A-register to receive data and the B-register to transmit data.

Cable Drivers and Terminators

A number of lines from the 1401 DPS circuitry terminate in a 200-position cable connector. Some of these lines are jumpered together inside the cable connector shoe to complete circuits within the 1401 DPS when the 7040-7044 DPS is utilized as the auxiliary unit on the 1401 DPS. By this means the 7040-7044 DPS controls its selected address, fixes its parity (odd or even), controls the order in which data are sent and received (high-order first; low-order last), controls the type of start-reset signal, and controls the fall of the service response line.

Because the 7040-7044 DPS can be located up to 100 feet from the 1401 DPS, line drivers and line terminators are required for all outgoing and incoming lines. Line drivers and terminators also allow for easy conversion of signals between units if the two units are designed with different types of circuitry. The conversion from one type of signal to another type is made by specifying the type of signal that must appear on all cable lines.

The output of the line driver when on forces 14 milliamperes of current through the cable. When the line driver is off, the line looks like an open circuit. This feature is desirable since everything is in an off condition if the cable is not connected to the system. The actual voltage swing on the line is determined by the resistor network associated with the line terminator at the other end of the cable.

Although the 1401 DPS ALD logic is shown as having in-phase outputs on the DT cards (CED-, P/N 370145), this and other DT type cards used in the 1401 DPS are actually out-of-phase outputs; that is, a -C input to the DT type card provides a + output and the line should be shown as an out-of-phase line rather than an in-phase line. These are shown in the proper phase relationship in this manual; therefore, they are the opposite of those shown in the 1401 DPS ALD logic.

1401 DPS CTDL Triggers

Although most of the circuits used in the 1401 DPS are considered to be standard circuits, there are some pecularities involving the CTDL triggers in the ALD logic. The CTDL trigger card (CW--, P/N 371534 and JZ--, P/N 371082) has normal inputs shown on the left-hand side of the card; however, some circuits used in the 1401 DPS ALD logic use "collector pullover" to set these triggers. It appears that the outputs of some of these triggers are tied to outputs from another card but are not connected in any other useful way. However, a closer look at Figure 49 shows that if a signal is applied to pins H or E, the trigger may be turned on by "collector pullover" rather than the normal inputs at B and A, G, C and D, or F.

The CW-- or the JZ-- trigger card consists of a CTDL trigger circuit designed for use as a single-bit memory device. The bi-stable circuit, consisting of two inverters and two emitter followers, operates at a frequency up to 250 kc. A positive CTDL signal applied to the ac set and gate (pins A and B) or to the dc set (pin G) controls the triggering action. Both in-phase and out-of-phase outputs are available from both cards.

DC Set Input: A positive T line applied to the dc set input causes the circuit to be triggered. Because of the circuit delays, the input pulse duration must be long enough to insure the latch-back condition of the trigger (minimum of 0.5 microseconds).

AC Set Input: When using the trigger as a single-bit memory device, both the signal input and the gate inputs are driven by CTDL U lines. The gate sets the reference threshold for the ac set input and must be conditioned 3.75 microseconds before the set signal is applied. If the gate is up, a +U line shift having a minimum pulse duration of 0.5 microsecond is required to reverse the condition of the trigger.

Circuit Description: Assume a starting condition of T4 and T2 conducting, and T3 and T1 off. When a +T level is applied to the dc set input (pin G), the base of T4 becomes more positive than the emitter (ground potential). T4 reverse-biased off causes its collector voltage to drop to -12v. This negative swing is coupled through C23 to forward-bias T3 on, and to T2 to decrease the conduction through the emitter follower (T2). Conduction through T3 causes its collector voltage to rise to 0 volt. This positive swing is coupled to T4 by C24 (keeping it cut off) and also to the base of T1. T1 becomes more forward-biased and conducts harder, causing the emitter-follower output (pin P) to increase to +2.7 volts. This up-level is latched back through D12 to keep T4 cut off. If a +T level is now applied to pin F (dc reset), the trigger is flipped to its original state. The positive level at pin F cuts off T3, causing its collector to drop to -12v. This negative shift is coupled through C24 to forward-bias T4 and drive it into conduction. The collector voltage of T4 goes to 0 volt, and allows the emitter-follower T2 to conduct more. The positive shift at the collector of T4 is also coupled through C23 to the base of T3 and holds it cut off. The

emitter-follower output at pin N (2.7 volts) is latched back through D11 to keep T3 cut off.

The turn-on and turn-off delays are a function of circuit loading and are noted above for nominal conditions. Over-all trigger delays in flipping from state to state average from 0.12 microsecond to 0.45 microsecond.

Also note that "collector pullover" is nothing more than a means of flipping the trigger by applying -12 volts to pin H in the first condition described, or to pin E in the second condition described. From this point, the description would be identical with the operations described previously.

1401 Serial I-O Adapter Location

The 1401 Serial I-O Adapter is located in gate 02A2 of the 1401 DPS, Models B, C, D, E, or F. The serial I-O adapter circuitry is designed to accommodate several different I-O devices; therefore, the 7040-7044 DPS uses only that portion of the serial I-O adapter circuitry that is necessary for the 7040-7044 DPS, 1401 DPS operations. If the 1401 DPS is a tape system, the first three rows of SMS cards in the 02A2 gate will be used for magnetic tape operations and for the serial I-O adapter.

1401 INSTRUCTIONS

1401 Instruction Modification for Serial I-O Adapter Operation

The 1401 DPS was designed to read and write magnetic tape; therefore, by changing the select address of the I-O instruction, the same instructions can be used to read data from the 7040-7044 DPS or to transmit data to the 7040-7044 DPS. Gating arrangements were added to transfer data into the A-register from the 7040-7044 DPS and to transmit data from the B-register of the 1401 DPS to the 7040-7044 DPS. In addition, a means was included of providing for control of 1401 DPS clock and signaling the 7040-7044 DPS that data was transmitted or received. Figure 52 shows the logic of this data flow between the 7040-7044 DPS and the 1401 DPS.

7040-7044 Address

Each auxiliary I-O unit attached to the 1401 DPS through the 1401 DPS Serial I-O Adapter has an assigned address. The assigned address for the 7040-7044 DPS is %A2.

M%A2BBBR (Move I-O Unit, Read)

The M%A2BBBR (move I-O unit, read) instruction is used to read information from the 7040-7044 DPS core storage into the 1401 DPS core storage. The data are transferred from the 7040-7044 DPS core storage to the storage bus, then to the storage register, and finally into the multiplier-quotient register. From the multiplier-quotient register, the data are transferred in six, six-bit characters to the A-register in the 1401 DPS, then through the inhibit mixing circuits into the 1401 DPS core storage.

A breakdown of the M%A2BBBR instruction format indicates that the M symbol is a move class of instruction. Word marks in the 1401 DPS core storage are not affected by the move operation. The %A2 symbol is the address assigned to the 7040-7044 DPS. The BBB symbol is the high-order position of the starting address in the 1401 DPS core storage into which the data from the 7040-7044 DPS will be read. The R symbol indicates a read instruction.

The read operation is completed when an end of transmission signal is received from the 7040-7044 DPS or when a group-mark word-mark is read from the 1401 DPS. A group-mark word-mark is comprised of bits WM, B, A, 8, 4, 2, 1. A group-mark is written into the 1401 DPS core storage when the end of transmission signal is received from the 7040-7044 DPS, and the group-mark indicates the end of the record to the 1401 DPS. Figures 53 and 55 show the group-mark forcing C, B, A, 8, 4, 2, 1 bits to be written into the A-register and stored in core storage.

M%A2BBBW (Move I-O Unit, Write)

The M%A2BBBW (move I-O unit, write) instruction is used to write information from the 1401 DPS core storage into the 7040-7044 DPS core storage. The data are transferred from the 1401 DPS core storage into the B-register. From the B-register the data are transferred to the multiplier-quotient register in the 7040-7044 DPS. When the multiplier-quotient register has received six, six-bit characters from the 1401 DPS, the multiplier-quotient register will be transferred to the storage register. Parity is checked and assigned upon the transfer of the data word into the storage register. From the storage register the data are transferred to the storage bus and into the 7040-7044 DPS core storage. The M symbol in the M%A2BBBW instruction signifies the operation is a move class of instruction in the 1401 DPS. The %A2 symbol is the assigned address of the 7040-7044 DPS. The BBB symbol is the high-order position of the starting address in the 1401 DPS core storage from which data will be read. The W symbol indicates the instruction transmits data from the 1401 DPS to the 7040-7044 DPS.

Word marks in the 1401 DPS core storage are not affected by the move class instructions. The write operation is completed when a group-mark word-mark is sensed in the 1401 DPS core storage

or when the 7040-7044 DPS word count is reduced to zero and the 7040-7044 DPS sends an end of transmission signal to the 1401 DPS.

L%A2BBBR (Load I-O Unit, Read)

The L%A2BBBR (load I-O unit, read) instruction reads information from the 7040-7044 DPS core storage into the 1401 DPS core storage. The data are transferred from the 7040-7044 DPS core storage to the storage bus, then to the storage register, and finally to the multiplier-quotient register. From the multiplier-quotient register, the data are transferred in six, six-bit characters to the A-register in the 1401 DPS and then into the 1401 DPS core storage.

A breakdown of the L%A2BBBR instruction format indicates that the L symbol is a load class instruction. The %A2 symbol is the assigned address of the 7040-7044 DPS and the BBB symbol is the high-order position of the starting address in the 1401 DPS core storage into which the data will be read. The R symbol indicates the data will be read from the 7040-7044 DPS and stored in the 1401 DPS.

Word marks in core storage are affected by the load instruction. When reading from the 7040-7044 DPS, a word mark in the 1401 DPS core storage is not regenerated. When a word separator (C, A, 8, 4, 1 bits) is read from the 7040-7044 DPS, the word separator will cause a word mark to be put into core storage with the next character that is read from the 7040-7044 DPS.

L%A2BBBW (Load I-O Unit, Write)

The L%2ABBBW (load I-O unit, write) instruction is used to write information from the 1401 DPS core storage into the 7040-7044 DPS core storage. The data are transferred from the 1401 DPS core storage into the B-register and then to the multiplier-quotient register in the 7040-7044 DPS. When the multiplier-quotient register has received six, six-bit characters from the 1401 DPS, the data in the multiplier-quotient register are transferred to the storage register. Parity is checked and assigned upon the transfer of the data word into the storage register. From the storage register the data are transferred to the storage bus and then to the 7040-7044 DPS core storage. In the L%A2BBBW instruction the L symbol signifies a load class instruction. The %A2 symbol is the assigned address of the 7040-7044 DPS. The BBB symbol is the high-order position of the starting address in the 1401 DPS core storage from which the data will be read. The W symbol indicates data are written from the 1401 DPS and read by the 7040-7044 DPS.

Word marks in core storage are affected by the load instructions. When writing to the 7040-7044 DPS, a word mark in any position causes a special character (word-separator, CA841) to be transferred to the 7040-7044 DPS prior to the character in that position. Thus, in effect, word marks are stored in the 7040-7044 DPS because only six data lines are used to transfer data between the 7040-7044 DPS and the 1401 DPS.

KA (I-O 1 Select)

The KA (I-O 1 select) instruction signals the 7040-7044 DPS that an error has occurred in the 1401 DPS program. The KA instruction causes a pulse from 060 to 000 time to be put on the I-O select 1 line (PC-142), Figures 50 and 51.

KB (I-O 2 Select)

The KB (I-O 2 select) instruction signals the 7040-7044 DPS that an end-of-file condition has occurred on the card reader or on a selected tape unit on the 1401 DPS. The KB instruction causes a pulse from 060 to 000 time to be put on the I-O 2 select line (PC-144), Figures 50 and 51.

KC (I-O 3 Select)

The KC (I-O 3 select) instruction signals the 7040-7044 DPS that an end-of-tape has occurred on a selected tape unit on the 1401 DPS. The KC instruction causes a pulse from 060 to 000 time to be put on the I-O 3 select line (PC-146), Figures 50 and 51.

KD (I-O 4 Select)

The KD (I-O 4 select) instruction signals the 7040-7044 DPS that an end-operation condition has been given by the 1401 DPS program. The KD instruction causes a pulse from 060 to 000 time to be put on the I-O 4 select line (PC-148), Figures 50 and 51, and the KD signal is used by the 7040-7044 DPS to end operation on a current select or control operation that has addressed the 1401 DPS.

KE (I-O 5 Select)

The KE (I-O 5 select) instruction signals the 7040-7044 DPS that the 1401 DPS program is in a loop. The 1401 DPS program, being in a loop, allows the 7040-7044 DPS to address the 1401 DPS with a select instruction. The KE instruction causes a pulse from 060 to 000 time to appear on the I-O 5 select line (PC-150), Figures 50 and 51.

KF (I-O 6 Select)

The KF (I-O 6 select) instruction signals the 7040-7044 DPS that the 1401 DPS attention instruction has been given by the 1401 DPS program. If the attention trap is enabled in the 7040-7044 DPS, the 7040-7044 DPS program will branch to a subroutine and acknowledge the 1401 DPS attention instruction. The KF instruction causes a pulse from 060 to 000 time to appear on the I-O 6 select line (PC-151), Figures 50 and 51.

K (AAA)d Signal Control and Branch Instructions

The K(AAA)d signal control and branch instructions are the same as the signal control instructions explained in the KA through KF series of instructions except that the next 1401 DPS program instruction will be taken from the core storage location beginning at the location specified by (AAA) in the signal control and branch instruction. The d portion of the signal control and branch instructions are the same as those listed in the signal control instructions (KA through KF).

B(AAA)1 Test and Branch

The B(AAA)1 test and branch instruction causes the 1401 DPS program to branch to the address specified in (AAA) if the set 1401 error latch signal (PC-086), Figures 50 and 51, has been executed by the 7040-7044 DPS. The set 1401 error latch signal is a result of a process check signal received from the 1401 DPS.

B(AAA)2 Test and Branch

The B(AAA)2 test and branch instruction causes the 1401 DPS program to branch to the address beginning at the location specified in the (AAA) portion of the test and branch instruction if the instruction waiting for 1401 line (PC-088), Figures 45 and 47, has been activated by a select (RDSA, PRDA, WRSA, PWRA, CTLA, SNSA, REWA, RUNA, BSRA, WEFA, or WBTA) instruction in the 7040-7044 DPS program. A select instruction addressing the 1401 DPS from the 7040-7044 DPS cannot end operation until the 1401 DPS acknowledges the select instruction with the KD instruction (except SNSA, 1401 not ready).

B(AAA)5 Test and Branch

The B(AAA)5 test and branch instruction causes the 1401 DPS program to branch to the address specified by the (AAA) portion of the test and branch instruction if the 1401 sense indicator line (PC-099), Figures 45 and 47, is active. The 1401 sense indicator line will be active (-C) when the SLNA (status line on, channel A) instruction has been performed by the 7040-7044 DPS program. The 1401 sense indicator line may be turned off by giving the SLFA (status line off, channel A) instruction or the reset channel (RDCA) instruction.

DATA AND CONTROL LINES

The 1401 DPS is connected to the 7040-7044 DPS channel A, interface 5, by a 200-position connector and interconnecting cable; Figures 43 and 44 show the 7040-7044 DPS to 1401 DPS interface lines. Several data and control lines are used to transfer data and control information between the two data processing systems. Not all of the lines that are terminated at the 200-position connector in the 1401 DPS are used by the 7040-7044 DPS or the 1401 DPS; therefore, only those lines that are used for input-output operations involving the 7040-7044 and 1401 DPS will be discussed. The cable reference number for the 200-position connector is 02TD; however, it is often referred to as PC. Plug connector locations conform to the following convention: 02TD-086 (PC-086) signal wire, and 02TD-087 (PC-087) reference wire, as shown under "Set 1401 Error Latch" for PC-086/087.

OUTPUT LINES

For purposes of discussion, the output lines are referred to as those lines having their line drivers in the 7040-7044 DPS and their line terminators in the 1401 DPS. Therefore, we will look at the function of each of the output lines as originating in the 7040-7044 DPS and sending some control or data information to the 1401 DPS. Each line name given is the line name as it appears in the 7040-7044 DPS. The 1401 DPS equivalent line name is given in the detailed description for each line.

Set 1401 Error Latch (PC-086/087)

The set 1401 error latch line is the I-O transfer 1 (error) line in the 1401 DPS. The set 1401 error latch line (Figures 50 and 51) is activated by the process check line (PC-095) from the 1401 DPS, and is gated by an interface 5 signal in the 7040-7044 DPS. The I-O transfer 1 line may be tested by the B(AAA)1 branch instruction in the 1401 DPS. If the condition is met; that is, a process check has occurred in the 1401 DPS program and the 7040-7044 DPS has gated the process check signal to the 1401 DPS, the 1401 DPS program will branch to the address location beginning being specified by (AAA) in the branch instruction. If a no-error condition is present, the 1401 DPS program will proceed to the next sequential instruction.

Instruction Waiting for 1401 (PC-088/089)

The instruction waiting for 1401 line is the I-O transfer 2 line in the 1401 DPS. The instruction waiting for 1401 line (Figures 45 and 47) is activated by the operate select level (ALD 03.10.01.1) and is a result of any select instruction (RDSA, PRDA, WRSA, PWRA SNSA, CTLA, WBTA, BSRA, WEFA, REWA, or RUNA) being decoded during I time in the 7040-7044 DPS. The operate select level is gated by an interface 5 and not sense busy signal before it is sent to the 1401 DPS (ALD 03.05.08.1). The I-O transfer 2 line may be tested by the B(AAA)2 branch instruction in the 1401 DPS program. If the condition is met, that is, an instruction is waiting for the 1401 DPS, the 1401 DPS program branches to the instruction beginning at the location specified by (AAA) in the branch instruction. If the condition is not met, the 1401 DPS program proceeds with the next sequential instruction.

1401 Sense Indicator (PC-098/099)

The 1401 sense indicator line is the I-O transfer 5 line in the 1401 DPS. The 1401 sense indicator line (Figures 45 and 47) is turned on by the status line on, channel A (SLNA) instruction in the 7040-7044 DPS. The 1401 sense indicator line may be turned off by the SLFA (status line off, channel A) instruction or by the RDHA instruction. The I-O transfer 5 line may be tested by the B(AAA)5 branch instruction in the 1401 DPS program. If the condition is met, that is, the SLNA instruction has turned on the 1401 sense indicator line in the 7040-7044 DPS, the 1401 DPS program branches to the address beginning at the location specified by (AAA) in the branch instruction. If the condition is not met, the 1401 DPS program proceeds to the next sequential instruction in its program.

1401 Sense Indicator Light (PC-134/135)

The 1401 sense indicator light line is the I-O error line in the 1401 DPS. The 1401 sense indicator light line (Figures 45 and 47) is activated by the SLNA (status line on, channel A) instruction in the 7040-7044 DPS program. The 1401 sense indicator light line may be turned off by the SLFA (status line off, channel A) instruction in the 7040-7044 DPS program or by the RDCA instruction. The I-O error line in the 1401 DPS is used to turn on the I-O error display light (ALD 34.33.13.2) and cannot be sensed by a branch instruction. The I-O transfer 5 line is activated by the same instruction.

End of Transmission (PC-091/092)

The end-of-transmission line is the end-of-transmission line in the 1401 DPS. The end-of-transmission line (Figures 45 and 47) is activated by an initial word count of zero during the 7040-7044 DPS program RCHA instruction, parity check enabled, or the end of message being sent to the 1401 DPS. During a 7040-7044 DPS write operation (1401 DPS read operation), the 7040-7044 DPS can turn on the end-of-transmission line when SC=0 and WC=0. The end-of-transmission line must remain on for a minimum of 12 microseconds during the 7040-7044 DPS write operation to insure proper termination of the 7040-7044 DPS write operation. During a 7040-7044 DPS read operation (1401 DPS write operation), the 7040-7044 DPS turns on the end-of-transmission line and causes the 1401 DPS to stop writing and proceed to the next sequential instruction in the 1401 DPS program. The end-of-transmission line must remain on for a minimum of 20 microseconds during the 7040-7044 DPS read operation to insure proper termination of the 7040-7044 DPS read operation.

SVC Response to 1401 (PC-113/114)

The SVC response to 1401 line is the service request line in the 1401 DPS. The SVC response to 1401 line is active during an instruction transfer to the 1401 DPS or during the time the 7040-7044 DPS requires service. The instruction transfer just mentioned is the result of any select instruction being decoded during I time in the 7040-7044 DPS that is addressing the 1401 DPS. The entire contents of the storage register are transferred to the multiplier-quotient register, the output mode trigger is set during I late time, and the shift counter is set to 6 at L2D1 time (Figures 45 and 47). If the 7040-7044 DPS is ready to send a character to the 1401 DPS or if it has received a character from the 1401 DPS and is ready to transmit or receive the next character, the SVC response to 1401 line is active.

When the SVC response to 1401 line is active, a response trigger in the 1401 DPS is reset (Figures 45 and 47) and the request trigger is set; the request trigger allows starting the 1401 DPS clock. The request trigger is reset by turning off the I-O selecting unit line from the 7040-7044 DPS. The SVC response to 1401 line must go to +C for a minimum of 2 microseconds before the request trigger can be set again.

I-O Selecting Unit (PC-132/133)

The I-O selecting unit line is the I-O selecting unit line in the 1401 DPS. The I-O selecting unit line (Figures 45 and 47) must be held at a -C level when

the 7040-7044 DPS is either sending or receiving data from the 1401 DPS. The I-O selecting unit line is conditioned by an interface 5 signal; when the interface 5 signal is reset at the following I time in the 7040-7044 DPS (next instruction), the service request trigger in the 1401 DPS is held off by the collector pullover input and cannot accept a service request signal.

Write Bus---to 1401 (PC-171 through 184)

The write bus (1,2,4,8,A,B,C) to 1401 lines are the I-O input (1,2,4,8,A,B,C) lines in the 1401 DPS. The write bus (1,2,4,8,A,B,C) to 1401 lines (Figures 45 and 47) are active when data are to be entered into the 1401 DPS. The 1401 DPS enters this data into its A-register during 000-030 time of a B-cycle when the I-O unit is selected and an I-O read call signal is given. PC numbers associated with each of the data lines are:

Write bus 1 to 1401	(PC-172/171)	I-O input 1
Write bus 2 to 1401	(PC-174/173)	I-O input 2
Write bus 4 to 1401	(PC-176/175)	I-O input 4
Write bus 8 to 1401	(PC-178/177)	I-O input 8
Write bus A to 1401	(PC-180/179)	I-O input A
Write bus B to 1401	(PC-182/181)	I-O input B
Write bus C to 1401	(PC-184/183)	I-O input C

INPUT LINES

For purposes of discussion, the input lines are referred to as those lines having their line drivers in the 1401 DPS and their line terminators in the 7040-7044 DPS. Therefore, look at the function of each of these lines as originating in the 1401 DPS and sending some control or data information to the 7040-7044 DPS. Each line name is the line name as it appears in the 7040-7044 DPS. The 1401 DPS equivalent line name is given in the description of each line.

1401 Is Stopped (PC-059/060)

The 1401 is stopped line is the 1401 is stopped line in the 1401 DPS. The 1401 is stopped line is active (-C) when the delta process latch in the 1401 DPS is off and the 1401 DPS is not executing an I-O operation. The 1401 is stopped line resets the 1401 ready trigger (Figures 50 and 51) in the 7040-7044 DPS.

1401 Start Reset Key (PC-084/085)

The 1401 start reset key line is the 1401 start reset key line in the 1401 DPS. The 1401 start reset key line is active (-C) when the 1401 start reset key is pressed in the 1401 DPS. The -C level is selected by a jumper (PC-039 to PC-038) in the 200-position connector rather than a +C level. When the 1401 start reset line is active, the 1401 ready trigger (Figures 50 and 51) in the 7040-7044 DPS is reset. When the 1401 start reset line goes off, the SVC response is gated to the 1401 DPS (Figures 4 and 5).

1401 Process Check (PC-095/105)

The 1401 process check line is the I-O process check line in the 1401 DPS. The 1401 process check line is at a -C level (Figures 50 and 51) when a process check (B-register, A-register, arithmetic, inhibit, op-register, or star error) exists in the 1401 DPS and the 1401 DPS serial I-O adapter has been selected by the 1401 DPS. The jumper between PC-007 and PC-022 is responsible for the gating of the 1401 process check line. The I-O process check line can be used to stop the 7040-7044 DPS. The 1401 process check line notifies the 7040-7044 DPS that the 1401 DPS will stop at the completion of the I-O operation if the 1401 process check switch is on, unless it is an A-register error. (A-register error is reset by I-O trans 1.)

1401 Service Request (PC-119/118)

The 1401 service request line is the service response line in the 1401 DPS. This line (Figures 45 and 47) is active (-C) from 030 time until the turn-on of the SVC response to 1401 line (PC-113) in the 7040-7044 DPS during an I-O read call from the 1401 DPS, or from 075 time until the turn-on of the SVC response to 1401 line in the 7040-7044 DPS during an I-O write call from the 1401 DPS. The 1401 service request line signals the 7040-7044 DPS that the 1401 DPS has taken the input data during a read operation by the 1401 DPS, or that the 1401 DPS has data available to the 7040-7044 DPS during a write operation. A group-mark word-mark encountered in the 1401 DPS core storage during a 1401 DPS write operation does not cause a 1401 service request signal to occur.

1401 Error Instruction KA(PC-142/141)

The 1401 error instruction KA line is the I-O 1 select line in the 1401 DPS. The 1401 error instruction KA line is active (-C), Figures 50 and 51, when a stacker select (K) code modified by character (A) has been executed by the 1401 DPS. The 1401 error instruction KA line is gated by a select interface 5 signal, and if the KA instruction and the select interface 5 signals are present, the 7040-7044 DPS recognizes that an error has occurred in the 1401 DPS.

1401 EOF Instruction KB (PC-144/143)

The 1401 EOF instruction KB line is the I-O 2 select line in the 1401 DPS. The 1401 EOF instruction KB

line is active (-C), Figures 50 and 51, when a stacker select (K) code modified by character (B) has been executed by the 1401 DPS. The 1401 EOF instruction KB line is gated by a select interface 5 signal. If the KB instruction and the select interface 5 signals are present, the 7040-7044 DPS sets the end-of-file trigger (Systems 03.30.04.1) and a normal operation follows; that is, it is the same as if the end-of-file trigger had been set by a signal from the 1414 I-O synchronizer instead of the 1401 DPS.

1401 EOT Instruction KC (PC-146/145)

The 1401 EOT instruction KC line is the I-O 3 select line in the 1401 DPS. The 1401 EOT instruction KC line is active (-C), Figures 50 and 51, when a stacker select (K) code modified by character (C) has been executed by the 1401 DPS. The 1401 EOT instruction KC line is gated by a select interface 5 signal; if the KC instruction and the select interface 5 signals are present, the 1401 DPS KC instruction sets the end-of-tape trigger (Systems 03.30.04.1) in the 7040-7044 DPS. Once the end-of-tape trigger has been set by the 1401 DPS, the sequence of operations is identical to the sequence following the setting of the end-of-tape trigger by a signal from the 1414 I-O synchronizer.

1401 End Op Instruction KD (PC-148/147)

The 1401 end op instruction KD line is the I-O 4 select line in the 1401 DPS. The 1401 end op instruction KD line is active (-C), Figures 50 and 51, when a stacker select (K) code modified by character (D) has been executed by the 1401 DPS. The 1401 end op instruction KD line is gated by a select interface 5 signal. If the KD instruction and the select interface 5 signals are present, the 1401 DPS KD instruction sets the 1401 end trigger and resets the 1401 ready trigger (Figures 50 and 51) in the 7040-7044 DPS. At the A2D1 pulse following the setting of the 1401 end trigger, a 1401 EOR signal occurs if the current instruction being performed in the 7040-7044 DPS is the RCHA instruction. If the present operation being performed in the 7040-7044 DPS is any select operation, a 1401 end select signal (Figures 50 and 51) occurs at A2D1 time following the setting of the 1401 end trigger.

1401 In Loop Instruction KE (PC-150/149)

The 1401 in loop instruction KE line is the I-O 5 select line in the 1401 DPS. The 1401 in loop instruction KE line is active (-C), Figures 50 and 51, when a stacker select (K) code modified by character (E) has been executed by the 1401 DPS. The 1401 in loop instruction KE line is not gated by an interface 5 signal; therefore, the 1401 ready trigger (Figures 50 and 51) is set when the KE instruction is executed by the 1401 DPS.

1401 Attention Instruction KF (PC-152/151)

The 1401 attention instruction KF line is the I-O 6 select line in the 1401 DPS. The 1401 attention instruction KF line is active (-C) (Figures 50 and 51) when a stacker select (K) code modified by character (F) has been executed by the 1401 DPS. The attention sync trigger (Systems 03.05.06.1) is set as soon as the KF instruction is received in the 7040-7044 DPS. The 1401 attention trigger (Systems 03.05.06.1) is set if the attention sync trigger is set and a trap sample is initiated by the 7040-7044 DPS. If the attention has been enabled, a 1401 attention and enable signal occurs and a trap routine can be executed by the 7040-7044 DPS program.

Read Bus---from 1401 (PC-186 through 199)

The read bus (1,2,4,8,A,B,C) from 1401 lines are the I-O output (1,2,4,8,A,B,C) lines in the 1401 DPS. The read bus (1,2,4,8,A,B,C) from 1401 lines are at -C when they contain information to be entered into the 7040-7044 DPS multiplier-quotient register bit positions 30 through 35 (Figures 45 and 47). The read bus (1,2,4,8, A,B,C) from 1401 lines are active from 060 to 090 time or from 060 time until the fall of the service response, whichever remains up the longest when the lines contain information and the 1401 I-O write call line is on. The read bus (1,2,4,8,A,B,C) from 1401 lines are fed from the B-register in the 1401 DPS. The B-register is reset from 000 to 015 time and set from 000 to 030 time. The data can be taken from the read bus (1,2,4,8,A,B,C) 1401 lines after 060 time of a 1401 B-cycle. The connectors and the lines they represent are:

Read bus 1 from 1401	(PC-186/187)	I-O output 1
Read bus 2 from 1401	(PC-188/189)	I-O output 2
Read bus 4 from 1401	(PC-190/191)	I-O output 4
Read bus 8 from 1401	(PC-192/193)	I-O output 8
Read bus A from 1401	(PC-194/195)	I-O output A
Read bus B from 1401	(PC-196/197)	I-O output B
Read bus C from 1401	(PC-198/199)	I-O output C

1401 INTERCONNECTION JUMPER LINES

Fifty-four output lines are terminated in the 200-position connector located in the 1401 DPS. These 54 output lines do not have cable drivers connected to them; they are used to complete circuits within the 1401 DPS by jumpering certain combinations of these lines together in the 200-position connector. The jumpers must be installed in the 200-position connector

and cannot be done in the 7040-7044 DPS itself. Not all 54 output lines are utilized when the 1401 DPS is connected as an auxiliary unit to the 7040-7044 DPS. Those lines that are important to 7040-7044, 1401 DPS operation are described on the following pages. The description is in numeric order, and where the line has been discussed earlier because the previous line was jumpered to this line, a notation to check some previous PC number is used. Figure 41 shows a layout of the I-O attachment connector receptacle.

A-Reg Sel 1 (PC-001)

The character (N) that addresses the 7040-7044 DPS is located in the A-register at I ring 2 time in the 1401 DPS. The output of the A-register must be jumpered in the I-O cable connector to select the 7040-7044 DPS. The A-reg sel 1 line is jumpered to the A-reg AB line (PC-017) as one of the three necessary conditions to provide the address of %A2 assigned to the 7040-7044 DPS. Figures 45 and 47 show the other necessary conditions: not A-reg 84, A-reg 1 not 2, unit select, and time 090 to 000.

A-Reg Sel 2 (PC-002)

The character (N) that addresses the 7040-7044 DPS is located in the A-register at I ring 2 time. The output of the A-register must be jumpered in the I-O cable connector to select the 7040-7044 DPS. The A-reg sel 2 line is jumpered to the A-reg 1 not 2 line (PC-035) as one of the three necessary conditions for selecting the %A2 address assigned to the 7040-7044 DPS. Figures 45 and 47 show the other conditions necessary to select the 7040-7044 address: A-reg AB, not A-reg 84, unit select, and time 090 to 000.

A-Reg Sel 3 (PC-003)

The character (N) that addresses the 7040-7044 DPS is located in the A-register at I ring 2 time. The output of the A-register must be jumpered in the I-O cable connector to select the 7040-7044 DPS. The A-reg sel 3 line is jumpered to the A-reg not 84 line (PC-033) as one of the three necessary A-register conditions for selecting the %A2 address assigned to the 7040-7044 DPS. Figures 45 and 47 show the other conditions that are necessary for the %A2 address: A-reg AB, not A-reg 84, unit select, and time 090 to 000.

Force Odd Redundancy (PC-004)

The 7040-7044 DPS has odd-redundancy parity; therefore, the force odd redundancy line must be jumpered to force odd redundancy 1 out line (PC-019), Figures 45 and 47, for correct parity transmission between the 7040-7044 and 1401 DPS. The jumper between PC-004 and PC-019 allows setting the redundancy latch (ALD 70.61.31.2) when the %A2 address sets the select I-O latch (ALD 73.11.11.2).

Select I-O Attach Out (PC-007)

The 7040-7044 DPS controls the I-O process check output line during 7040-7044, 1401 DPS operations. If a read binary tape instruction is addressed to the 1401 DPS by the 7040-7044 DPS program and a BCD tape-mark is read on the selected tape unit on the 1401 DPS, a process check is sent to the 7040-7044 DPS under normal conditions. However, the BCD tape-mark on the tape is not a true error; the 1401 process check is inhibited by jumpering the select I-O attach out line to the select I-O attach in line (PC-022).

Reset A-Reg Error (PC-008)

If a transmission error occurs, it is desirable that the 7040-7044 DPS resets the A-register error. To accomplish this resetting, the reset A-reg error line must be connected to the reset A-reg error line (PC-023).

Set Error Latch In (PC-011)

When a set 1401 error latch signal is recieved (PC-086) from the 7040-7044 DPS by the 1401 DPS, and the B(AAA)1 branch instruction has not yet recognized that the error condition signal is present in the 1401 DPS, it is desirable that the condition be stored by setting the I-O error latch (Figures 45 and 47). To set the I-O error latch, the I-O error latch in line must be connected to the I-O error latch 1 out line (PC-026).

I-O Transfer EOR (PC-012)

Since neither the I-O transfer 1 nor the I-O transfer 2 line is used to give an I-O transfer end-of-record, the I-O transfer EOR line must be connected to +6 volts at PC-036 to prevent a false end-of-record from occurring when the select I-O attach line (ALD 73.11.31.2), Figure 45, is active.

A-Reg AB (PC-017)

For detailed description, see PC-001.

Force Odd Redundancy 1 Out (PC-019)

For detailed description, see PC-004.

Select I-O Attach In (PC-022)

For detailed description, see PC-007.

Reset A-Reg Error 1 (PC-023)

For detailed description, see PC-008.

I-O Error Latch 1 Out (PC-026)

For detailed description, see PC-011.

A-Reg Not 48 (PC-033)

For detailed description, see PC-003.

A-Reg 1 Not 2 (PC-035)

For detailed description, see PC-002.

+6 Volts (PC-036)

For detailed description, see PC-012.

Start Reset In (PC-038)

The 7040-7044 DPS requires an active (-C) level when the 1401 start-reset key is pressed; therefore, the start reset in line (Figure 50), must be connected to the start reset out line (PC-039) to meet the requirements for the 7040-7044 DPS start reset line to be at -C when active.

Start Reset Out (PC-039)

For detailed description, see PC-038.

Data C Out (PC-040)

The word-mark line is not used in the transfer of data between the 7040-7044 DPS and the 1401 DPS. The data C out line must be jumpered to the data C load or move in line (PC-049) to allow for the correct generation of the C-bit on the load or move operation in the 1401 DPS.

Service Request Out 1 (PC-041)

The 7040-7044 DPS requires the 1401 service response trigger to be turned off when the service request input signal (PC-113) is turned on. The service request out 1 line is jumpered to the service request in line (PC-043) to achieve the desired resetting of the 1401 service response trigger (ALD 73.11.71.2), Figure 45.

Service Request In 1 (PC-043)

For detailed description, see PC-041.

Select I-O Out (PC-046)

When any I-O device is attached to the 1401 DPS, the select I-O out line must be connected to select I-O in (PC-047), Figure 45. The select I-O out line is used to set the I-O select latch (ALD 73.11.11.2) when the address for the 7040-7044 DPS is in the A-register at I ring 2 time. The I-O select latch is set during 090 to 000 time of I ring 2 time.

Select I-O In (PC-047)

For detailed description, see PC-046.

Data C Load or Move In (PC-049)

For detailed description, see PC-040.

I-O Write Call In (PC-050)

The I-O write call in line must be jumpered to the I-O write call out line (PC-051), Figure 45, to enable the clock to start automatically on the first I-cycle when the select I-O attach line is active.

I-O Write Call Out (PC-051)

For detailed description, see PC-050.

7040-7044 AND 1401 DPS SYNCRHONIZATION

To start an input-output operation, the 7040-7044 DPS must be synchronized with the 1401 DPS. Synchronization can be obtained by several means, depending on the priority of the instruction and data to be transferred. Priority is determined by how soon the information is needed and how soon the data can be transferred.

If it is desired to call the immediate attention of the 1401 DPS, the status line on, channel A (SLNA) instruction sets the 1401 indicator trigger (Figure 45). The 1401 indicator trigger's output conditions the 1401 sense indicator line PC-099 (Figure 45) and the 1401 sense indicator light line (PC-134). The 1401 sense indicator line is the I-O transfer 5 line in the 1401 DPS. When the 1401 DPS program performs the B(AAA)5 branch instruction, the I-O transfer 5 line is tested; if the I-O transfer 5 line is on, the 1401 DPS program branches to the instruction beginning at the high-order position in the location specified by (AAA) of the branch instruction.

The program beginning at the location specified by (AAA) in the branch instruction can be the KF (1401 attention) instruction or the KE (1401 in loop) instruction. The instruction that is used depends on the prevailing conditions. If the 7040-7044 DPS is conditioned to allow a trap condition for the 1401 DPS, the KF (1401 attention) instruction can be executed by the 1401 DPS. When the 1401 attention trap is enabled in the 7040-7044 DPS, the KF instruction allows a transfer trap to a subroutine. If the 1401 attention trap has not been enabled in the 7040-7044 DPS, the KE (1401 in loop) instruction should be used. The KE instruction sets the 1401 ready trigger (Figure 50) in the 7040-7044 DPS. The 1401 ready trigger can be sensed by the 7040-7044 DPS TDOA instruction. If the 1401 ready trigger is on, the 7040-7044 DPS program executes the next sequential instruction when the TDOA instruction is given. If the 1401 ready trigger is off, the TDOA instruction causes the 7040-7044 DPS program to branch to the instruction at the address specified by bits 21 through 35 of the TDOA in struction.

In the methods of initial synchronization just described, assume the same subroutine is used for both conditions; that is, the TDOA instruction and the trap routing come to the same routine in the 7040-7044 DPS program. Since the initial input-output sequence began with the 7040-7044 DPS, assume a select instruction(RDSA, PRDA, WRSA, PWRA, CTLA WBTA, SNSA, REWA, RUNA, BSRA, WEFA) is to be sent to the 1401 DPS. When the 7040-7044 DPS executes the select instruction, the instruction waiting for 1401 line (PC-088), Figures 45 and 47, becomes active (-C) after I3D2 time when the instruction is decoded and the interface has been selected. The storage register (the current select instruction) is transferred to the multiplier-quotient register, the 1401 out-mode level becomes active, the out-mode trigger is set, and the shift counter is set to 6. Figure 46 shows an initial timing sequence for the select instruction; Figure 48 shows the initial timing sequence for the SLNA instruction.

The instruction waiting for 1401 line resets the I-O select 1 trigger (Figures 45 and 47) in the 1401 DPS; when the 1401 DPS program performs the B(AAA)2 instruction, the 1401 DPS program branches to the location specified by (AAA) of the branch instruction. The program beginning at the high-order position specified by the (AAA) portion of the branch instruction should select the 7040-7044 DPS (1401 DPS serial I-O adapter, address %A2), read six characters of data (the current select instruction), execute the KD instruction to allow the 7040-7044 DPS to end operation on its current select instruction, and then determine which select instruction was received from the 7040-7044 DPS. The 7040-7044 DPS cannot proceed to the next instruction until the KD instruction has been given by the 1401 DPS to allow an end-operation signal to be sent to the 7040-7044 DPS to end operation on the current select instruction in the 7040-7044 DPS.

Another method of initial synchronization could occur if the 7040-7044 DPS were to execute any of the select instructions addressing the 1401 DPS on channel A, interface 5. The select instruction causes the instruction waiting for 1401 line (PC-088), Figures 45 and 47, to become active. The contents of the storage register (the current select instruction) are transferred to the multiplier-quotient register, the out-mode trigger is set, and the shift counter is set to 6. No further operations can take place in the 7040-7044 DPS until the 1401 DPS program initiates a routing to read in the six characters of data from the 7040-7044 DPS and performs the KD (end operation) instruction to signal the 7040-7044 DPS that the current select instruction has been read into the 1401 DPS core storage and there is no further need of this data.

The B(AAA)2 branch instruction senses the I-O transfer 2 (instruction waiting for 1401) line, Figures 45 and 47. If an instruction is waiting, the 1401 DPS program branches to the location beginning at the high-order bit position specified by (AAA) in the branch instruction. The subroutine beginning at the high-order bit position location specified by (AAA) should read the current select instruction from the 7040-7044 DPS.

Other methods of synchronization are possible, beginning with the 1401 DPS requesting the use of the 7040-7044 DPS. The 1401 DPS can execute the KF (1401 attention) instruction, and if the 1401 attention trap is enabled in the 7040-7044 DPS, a trap occurs. The 7040-7044 DPS stores its instruction counter and branches to a subroutine. The subroutine could execute the RDSA instruction and read the information from the 1401 DPS; the 7040-7044 DPS can decide what operation is desired by the 1401 DPS and if data are to be transmitted or received by the 1401 DPS. The 7040-7044 DPS must initiate the proper action to comply with the request that was received from the 1401 DPS. The RDSA instruction addressing the 1401 DPS would be the same as that just described, except that the 1401 DPS was the unit to initiate the original input-output request.

Another method of input-output synchronization occurs when the 1401 DPS initiates the KE (1401 in loop instruction) and sets the 1401 ready trigger (Figures 50 and 51). The 1401 ready trigger must be sensed with the TDOA instruction in the 7040-7044 DPS program; an RDSA instruction must be initiated by the 7040-7044 DPS to read the information from the 1401 DPS, then the 7040-7044 DPS should proceed to a subroutine to determine what operation has been requested by the 1401 DPS or what action is required.

The KE instruction also informs the 7040-7044 DPS that the 1401 DPS is waiting for an instruction. In this case, the TDOA instruction could branch to a subroutine and execute a select instruction. The select instruction is sensed by the B(AAA)2 instruction in the 1401 DPS loop program. At this point, the routine depends on the select instruction given by the 7040-7044 DPS.

The examples given of synchronizing the 7040-7044, with the 1401 DPS for instruction and data transfers are only a few of the many available means of synchronization.

7040-7044 DPS Read Operation to the 1401 DPS

For purpose of discussion, assume the 7040-7044 DPS is in synchronization with the 1401 DPS, the current instruction is the RDSA instruction addressing the 1401 DPS, and the 1401 DPS has executed a subroutine and has determined that the 7040-7044 DPS has requested information from the 1401 DPS. Recall from the preceding discussion that the 1401 DPS system recognized the instruction waiting for 1401 signal by the B(AAA)2 branch instruction or some other appropriate method of synchronization. The 1401 DPS has addressed the 7040-7044 DPS (1401 DPS serial I-O adapter) and six, six-bit characters have been read. At the termination of the RDSA instruction (the 1401 DPS executed the KD instruction), the 7040-7044 DPS proceeds to the RCHA instruction. The RCHA instruction addresses the 7040-7044 DPS core storage for the IORD word and the word is transferred to the accumulator. The IORD contains the starting address in the 7040-7044 DPS core storage that information is read into and the number of words that are to be read from the 1401 DPS.

Since the 7040-7044 DPS has given the RDSA instruction, the 1401 DPS must give either the M%A2BBBW (move I-O unit, write) instruction or the L%A2BBBW (load I-O unit, write) instruction. The instruction that is used depends on whether the word marks are effected in the transfer.

The 1401 DPS write operation consists of selecting the 7040-7044 DPS (1401 DPS serial I-O adapter, address %A2), sending data to the 7040-7044 DPS, and terminating the write operation. When the 1401 DPS selects the 7040-7044 DPS, the select I-O attach line (Figure 45) is active at 090 time, and remains active until the completion of the write operation. The I-O write call line remains active because of the jumper that is installed between PC-050 and PC-051 in the 200-position connector. The I-O write call line does not become inactive until the request trigger (Figures 45 and 47) is reset by dropping the I-O selecting unit (PC-132) line to the 1401 DPS, thus resetting the request trigger. The write call line comes up during the I-cycle and causes the 1401 DPS to take one B-cycle. The 1401 DPS clock stops at the end of that cycle and waits until the 7040-7044 DPS brings up the service response to 1401 line (PC-113), Figures 45 and 47. If the service request trigger (Figures 45 and 47) was conditioned before the 1401 DPS clock stopped, the 1401 DPS continues to take B-cycles at an 86 kc rate; that is, a character is read into the 1401 DPS core storage every 11.5 microseconds. The service request trigger is gated with the write call signal and the select I-O signal to start the 1401 DPS clock. The data from the 1401 DPS core storage are available on the data lines at 060 time of the 1401 DPS B-cycle, and the data remain on the data lines until 090 time of the B-cycle or until the fall of the service response (whichever remains up the longest). If the 1401 DPS is stopped when the service request line becomes active, it will take from 2 to 5 microseconds to start the 1401 DPS clock. The 1401 DPS then takes a B-cycle and the information from core storage is set into the B-register by 030 time of the B-cycle. Once the information has been set in the B-register, it is available on the data lines to the 7040-7044 DPS at 060 time of the B-cycle. The 1401 DPS generates a service response signal at 075 time during a write call B-cycle. The 7040-7044 DPS can use the service response (1401 service request, PC-119) to indicate that the 1401 DPS has taken a cycle and has data waiting to be read on the data lines. The 1401 service request initiates a normal service request cycle in the 7040-7044 DPS; the 1401 DPS is synchronized with the 7040-7044 DPS and the data on the read bus (1,2,4,8,A,B,C)from 1401 lines are transferred into bit positions 31 through 35 of the multiplier-quotient register during the service request cycle. At sync 2 time in the 7040-7044 DPS, the output response trigger (Figure 5) is set, and the output of the output response trigger initiates an SVC response to 1401 signal (PC-113) to the 1401 DPS. The SVC response to 1401 signal resets the response trigger and sets the request trigger in the 1401 DPS.

The 1401 DPS clock stops after taking one B-cycle unless the SVC response to 1401 line is brought up again. The operation continues in this manner at a maximum rate of one character every 11.5 microseconds until the 1401 DPS write operation (7040-7044 DPS read operation) is terminated.

The 1401 DPS write operation is terminated when one of the following conditions occurs: (1) during a B-cycle, if the 1401 DPS reads a group-mark word-mark from the 1401 DPS core storage. The group-mark word-mark brings up the I-O disconnect line, drops the write call line at the end of the B-cycle, and starts to read the next instruction from the 1401 DPS core storage. (2) If the 7040-7044 DPS brings up the end-of-transmission line, the 1401 DPS terminates the write operation and proceeds to the next 1401 DPS program instruction. Figure 53 shows the

conditions for write call in the 1401 DPS. The end-of-transmission line (PC-091), Figure 45, is brought up when the word count is reduced to zero and the shift counter is zero. If an error condition occurs during the write operation, the 1401 DPS stops at the completion of the write operation. If an op-reg or star error occurs, the 1401 DPS stops at the completion of that cycle and drops the write call line that prevents any further transmission of data to the 7040-7044 DPS.

7040-7044 DPS Write Operation to the 1401 DPS

For the purposes of discussion, assume that the 7040-7044 DPS is in synchronization with the 1401 DPS; the current instruction is the WRSA instruction addressing the 1401 DPS on channel A, interface 5. Recall that the 1401 DPS has addressed the 7040-7044 DPS (1401 DPS serial I-O adapter, address %A2), the 1401 DPS has read six, six-bit characters (the current WRSA instruction) and has determined that the 7040-7044 DPS wishes to transmit data to the 1401 DPS. For the current WRSA instruction to be terminated, the 1401 DPS must have executed the KD (end-operation) instruction to the 7040-7044 DPS.

The 7040-7044 DPS proceeds to the RCHA instruction after the termination of the WRSA instruction. The KD instruction is necessary to allow the WRSA instruction to end operation. The RCHA instruction obtains the IORD word from the 7040-7044 DPS core storage and transfers it to the accumulator. The IORD contains information to instruct the 7040-7044 DPS to transmit the number of words specified by the word count of the IORD word and the starting location from which data will be transferred in the 7040-7044 DPS core storage.

When the 1401 DPS has determined the operation is a write instruction, the 1401 DPS has to execute either the M%A2BBBR (move I-O unit, read) instruction or the L%A2BBBR (load I-O unit, read) instruction. The 1401 DPS read operation consists of selecting the 7040-7044 DPS, reading data from the multiplier-quotient register in six-bit characters, and terminating the read operation at a given time. When the 1401 DPS selects the 7040-7044 DPS, the select I-O attach line (ALD 73.11.11.2) is active at I ring 2 time and remains active until I ring op time of the next 1401 DPS instruction. During the last instruction cycle of the I-O read operation, the I-O read call line (ALD 73.11.11.2) is active at 090 time and remains active until the completion of the read operation.

When the read call line becomes active during the I-cycle, the 1401 DPS clock stops at the end of the cycle and waits until the 7040-7044 DPS brings up the SVC request to 1401 line (PC-113), Figure 45. If the service request trigger was conditioned before the 1401 DPS clock stopped, the 1401 DPS requests another B-cycle; the service request line is gated with a read call signal to start the 1401 DPS clock. The 1401 DPS samples the I-O data lines from the 7040-7044 DPS, and the data are stored in the A-register during 000-030 time of the 1401 DPS cycle. The 7040-7044 DPS can use the SVC request to 1401 line as an indication that the 1401 DPS has taken a cycle. The service response line is activated and the service request trigger in the 1401 DPS is reset at 030 time. The data in the A-register are put into the 1401 DPS core storage during 065 to 000 time of the B-cycle. The 1401 DPS clock stops unless the SVC request to 1401 line has been activated by the 7040-7044 DPS, informing the 1401 DPS that new data have been transferred from the multiplier-quotient register. The SVC request to 1401 line should be active at this time under normal operating conditions. The data transfer continues in this manner at a maximum rate of one character every 11.5 microseconds until the read operation is terminated. The 1401 DPS read operation (7040-7044 DPS write operation) may be terminated by any of the following conditions: (1) During any B-cycle, a group-mark word-mark being read from the 1401 DPS core storage into the B-register brings up the I-O disconnect line for approximately 6 microseconds. A group-mark word-mark is stored in the selected core location instead of the character in the A-register that has just been received from the 7040-7044 DPS. The read call line becomes inactive at the end of this cycle and the next sequential instruction is read out of the 1401 DPS core storage. (2) If, at the completion of any B-cycle, the 7040-7044 DPS brings up the end-of-transmission line, the 1401 DPS takes one additional cycle and stores a group mark into the next 1401 DPS core storage location. The read call line becomes inactive at the end of this cycle and the next sequential instruction is read out of the 1401 DPS core storage. The end-of-transmission line should not be brought up until after the 1401 DPS has put the last character of information that it has received from the 7040-7044 DPS into its core storage. If the end-of-transmission line is brought up during the last character cycle, the A-register is reset from 045 to 075 time and a group mark is stored in the selected location, and the last character received from the 7040-7044 DPS is lost.

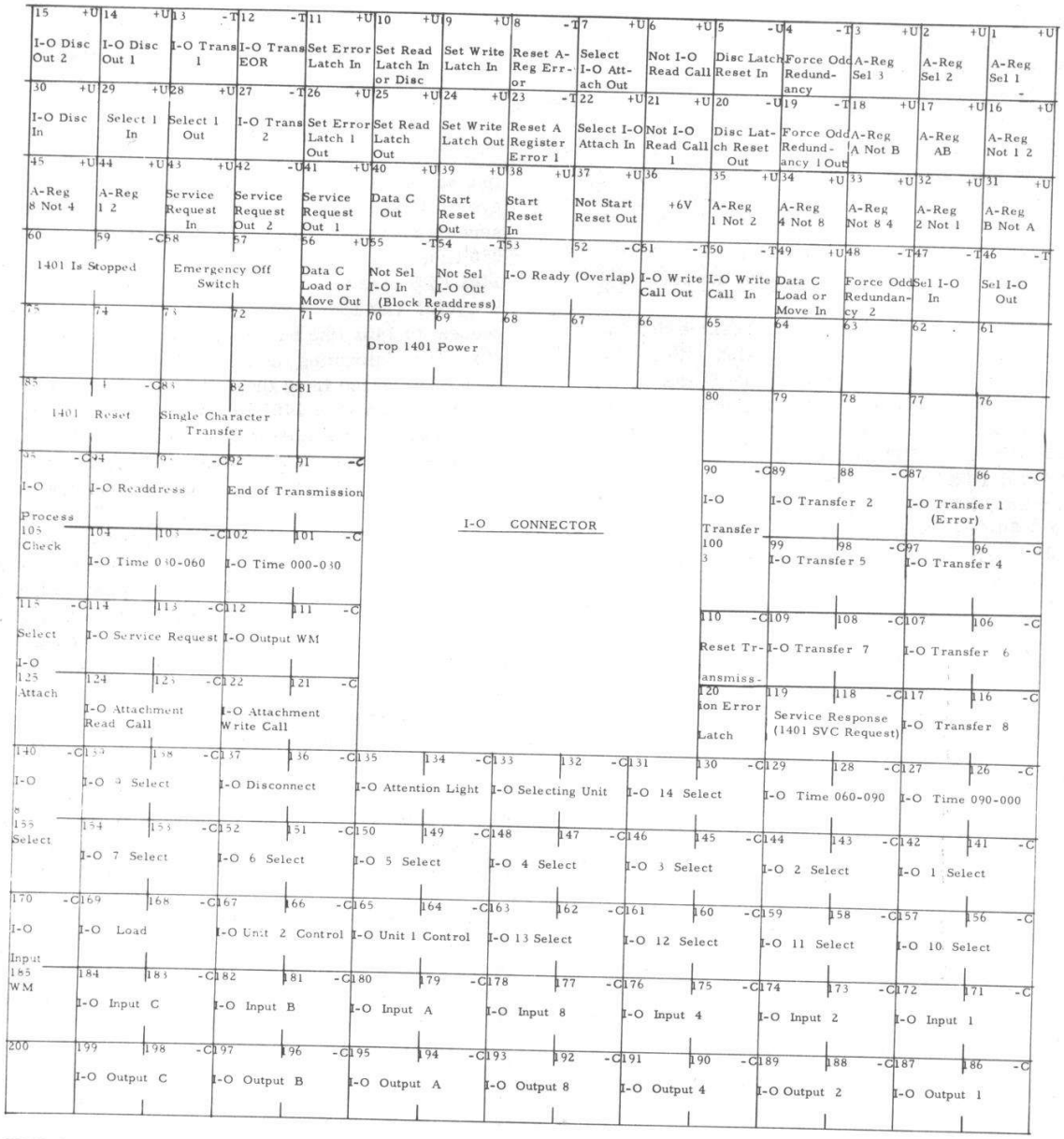
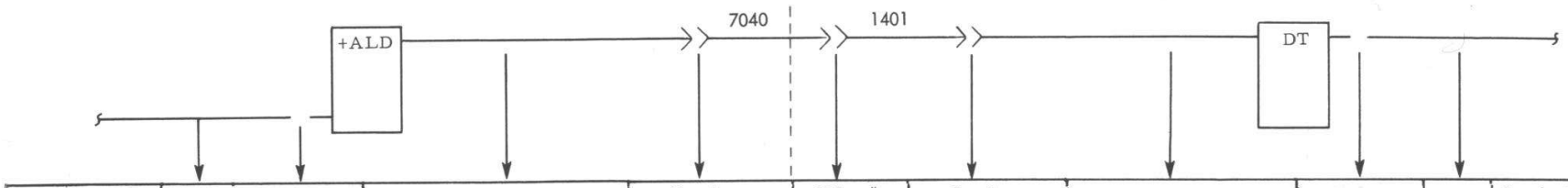
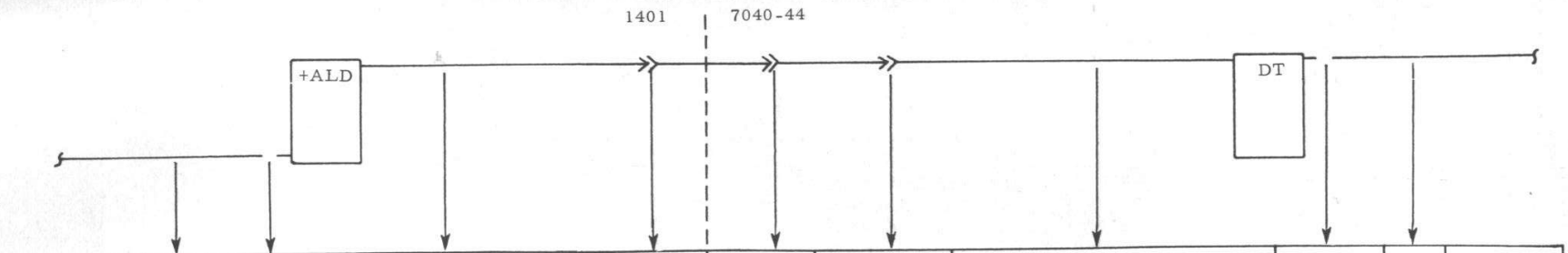


FIGURE 42. 1401 I-O ATTACHMENT CONNECTOR RECEPTACLE (CONNECTOR SIDE)



Logic Page	Line In	Input	CPU Line Name	Card Conn	PC #	Card Conn	1401 Line Name	Output	Line Out	Logic Page
03.05.01.1	+B	01E3J14S	-C Write Bus C to 1401	01E3L12P	PC-184	02A2E23J	-C I-O Input C	02A2D21E	+U	73.11.21.2
		01E3J14L	-C Write Bus B to 1401	01E3L12M	PC-182	02A2E23H	-C I-O Input B	02A2D21F		
		01E3J14P	-C Write Bus A to 1401	01E3L12K	PC-180	02A2E23G	-C I-O Input A	02A2D21D		
		01E3J14B	-C Write Bus 8 to 1401	01E3L12H	PC-178	02A2E23F	-C I-O Input 8	02A2D21P		
		01E3J14D	-C Write Bus 4 to 1401	01E3L12F	PC-176	02A2E23E	-C I-O Input 4	02A2D20E		
		01E3J14Y	-C Write Bus 2 to 1401	01E3L12D	PC-174	02A2E23D	-C I-O Input 2	02A2D20F		
03.05.01.1		01E3J144	-C Write Bus 1 to 1401	01E3L12B	PC-172	02A2E23C	-C I-O Input 1	02A2D20P		73.11.21.2
03.05.02.1		01E3J146	-C Set 1401 Error Latch	01E3L13M	PC-086	02A2E23N	-C I-O Trans 1	02A2D22D		73.11.41.2
		01E3J14G	-C Inst Waiting for 1401	01E3L13P	PC-088	02A2E23P	-C I-O Trans 2	02A2D22F		73.11.41.2
		01E3J14V	-C SVC Response to 1401	01E3U12P	PC-113	02A2E23L	-C Service Request	02A2D22E		73.11.11.2
		01E3J06S	-C End of Transmission	01E3L13R	PC-091	02A2E23B	-C End of Trans	02A2D20D		73.11.31.2
		01E3J06U	-C I-O Selecting Unit	01E3U12R	PC-132	02A2E23M	-C I-O Selecting Unit	02A2D22P		73.11.11.2
		01E3J20B	-C 1401 Sense Indicator	01E3U14R	PC-099	02A2E24B	-C I-O Trans 5	02A2E21D		73.11.51.2
03.05.02.1	+B	01E3J20D	-C 1401 Sense Ind Light	01E3L14H	PC-134	02A2E24P	-C I-O Error Light	02A2F19F	+U	73.11.51.2

FIGURE 43. CPU TO 1401 DPS I F 5 LINES



Logic Page	Line In	Input	1401 Line Name	Card Conn	PC #	Card Conn	CPU Line Name	Output	Line Out	Logic Page
73.12.11.2	+U	02A2F20C	-C I-O Output C	02A2F24B	PC-198	01E3U13P	-C Rd Bus C From 1401	01E3J13A	-B	03.05.03.1
		02A2F21E	-C I-O Output B	02A2F24C	PC-196	01E3U13M	-C Rd Bus B From 1401	01E3J13D		
		02A2F21G	-C I-O Output A	02A2F24D	PC-194	01E3U13K	-C Rd Bus A From 1401	01E3J13B		
		02A2F21C	-C I-O Output 8	02A2F24E	PC-192	01E3U13H	-C Rd Bus 8 From 1401	01E3J13L		
		02A2F22E	-C I-O Output 4	02A2F24F	PC-109	01E3U13F	-C Rd Bus 4 From 1401	01E3J13P		
		02A2F22F	-C I-O Output 2	02A2F24G	PC-188	01E3U13D	-C Rd Bus 2 From 1401	01E3J13U		
73.12.11.2		02A2F22C	-C I-O Output 1	02A2F24H	PC-186	01E3U13B	-C Rd Bus 1 From 1401	01E3J13K		03.05.03.1
73.11.71.2		02A2D23P	-C Service Response	02A2E26Q	PC-119	01E3L13H	-C 1401 Service Request	01E3J12D		03.05.04.1
73.11.31.2		02A2D19E	-C I-O Process Check	02A2E26H	PC-095	01E3L13F	-C 1401 Process Check	01E3J12A		
73.11.31.2		02A2D18E	-C 1401 Reset	02A2E26K	PC-084	01E3L13D	-C 1401 Start Reset Key	01E3J072		
73.11.61.2		02A2E20P	-C I-O 1 Select	02A2E25J	PC-142	01E3U12B	-C 1401 Error Instruction KA	01E3J12G		
		02A2E20F	-C I-O 2 Select	02A2E25K	PC-144	01E3U12D	-C 1401 EOF Instruction KB	01E3J12L		
		02A2E20D	-C I-O 3 Select	02A2E25L	PC-146	01E3U12F	-C 1401 EOT Instruction KC	01E3J12P		
		02A2E22P	-C I-O 4 Select	02A2E25M	PC-148	01E3U12H	-C 1401 End Op Instruction KD	01E3J12U		
		02A2E22F	-C I-O 5 Select	02A2E25N	PC-150	01E3U12K	-C 1401 In Loop Instruction KE	01E3J12X		03.05.04.1
73.11.61.2		02A2E22D	-C I-O 6 Select	02A2E25P	PC-152	01E3U12M	-C 1401 Att Instruction KF	01E3J122		03.05.06.1
73.12.21.2	+U	02A2F20E	-C 1401 Is Stopped	02A2F24L	PC-059	01E3L13B	-C 1401 Is Stopped	01E3J132	-B	03.05.04.1

FIGURE 44. 1401 DSP TO CPU I F 5 LINES

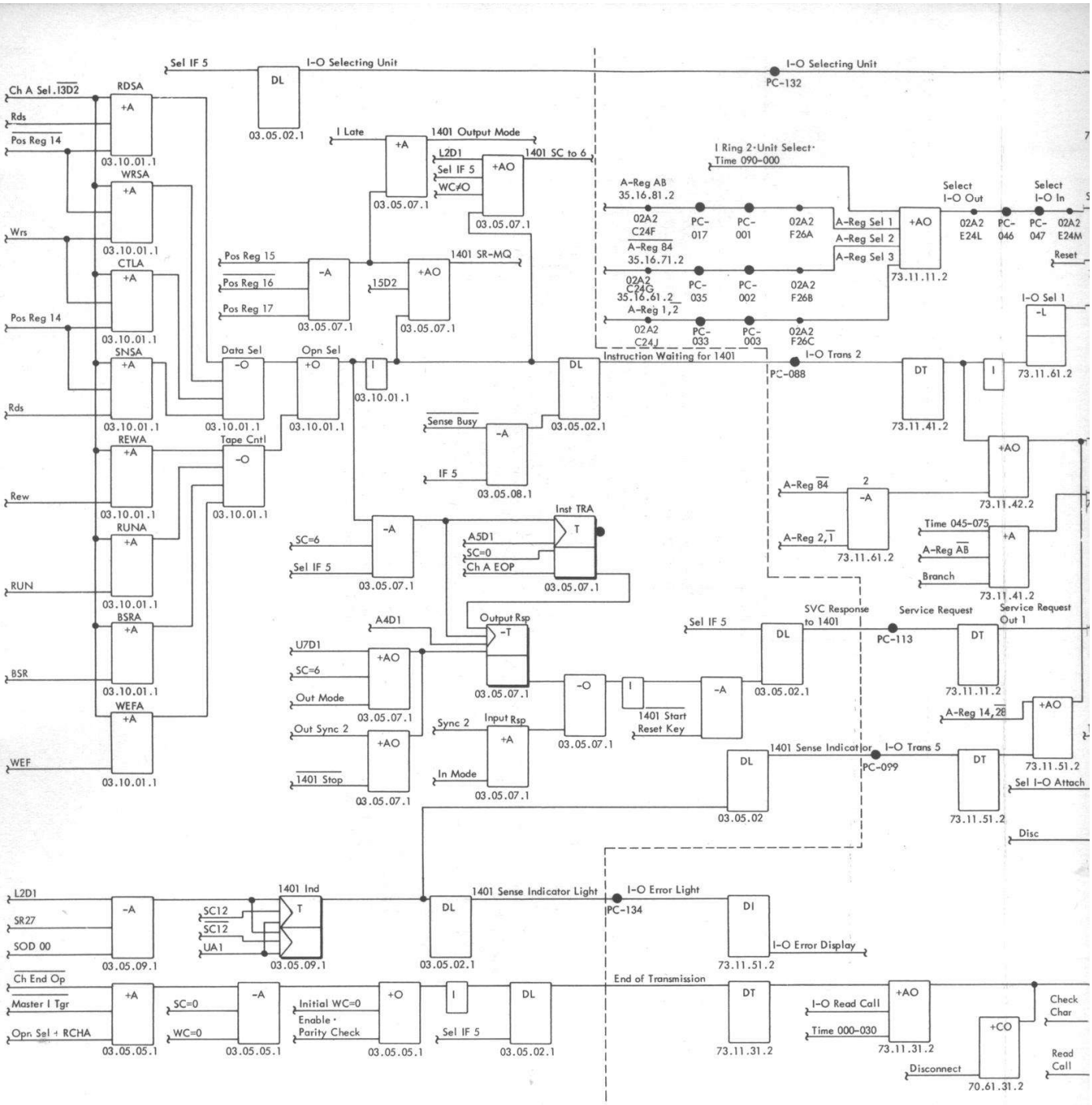
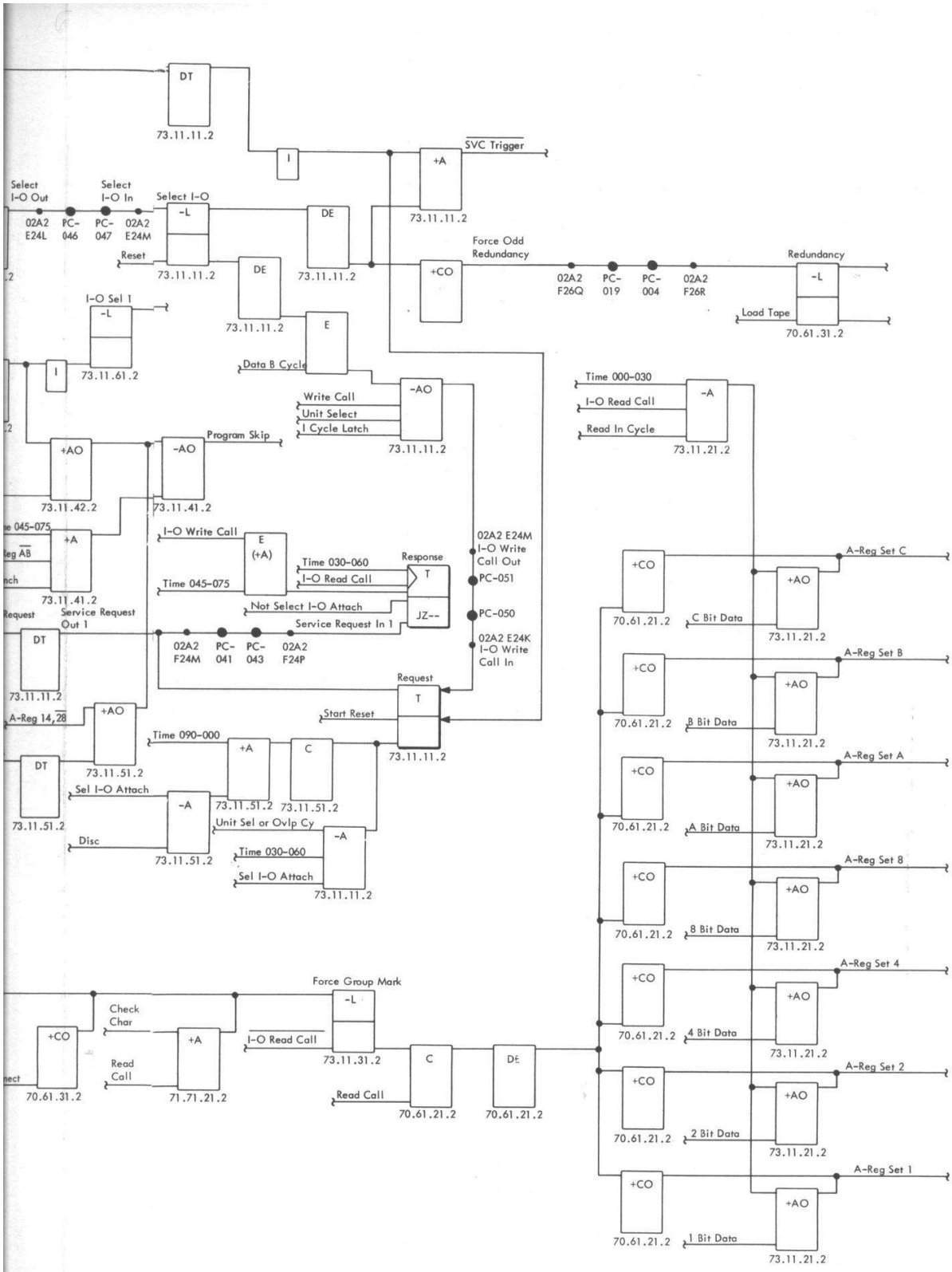


FIGURE 45. 7040-7044 SELECTION AND CONTROL; 2ND LEVEL ALD LOGIC



S23-5013 (223-2644) 12/9/63

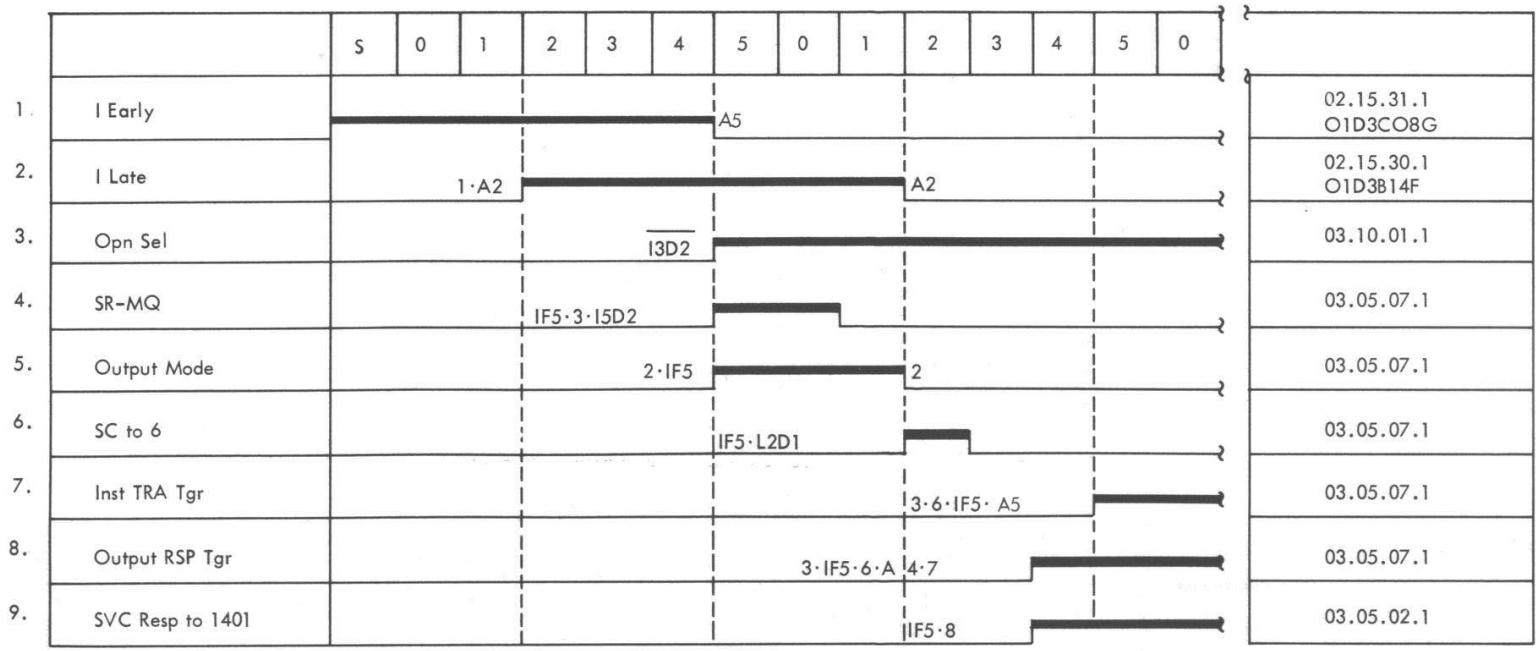


FIGURE 46. 7040-7044 TO 1401 SELECT INSTRUCTIONS TIMING

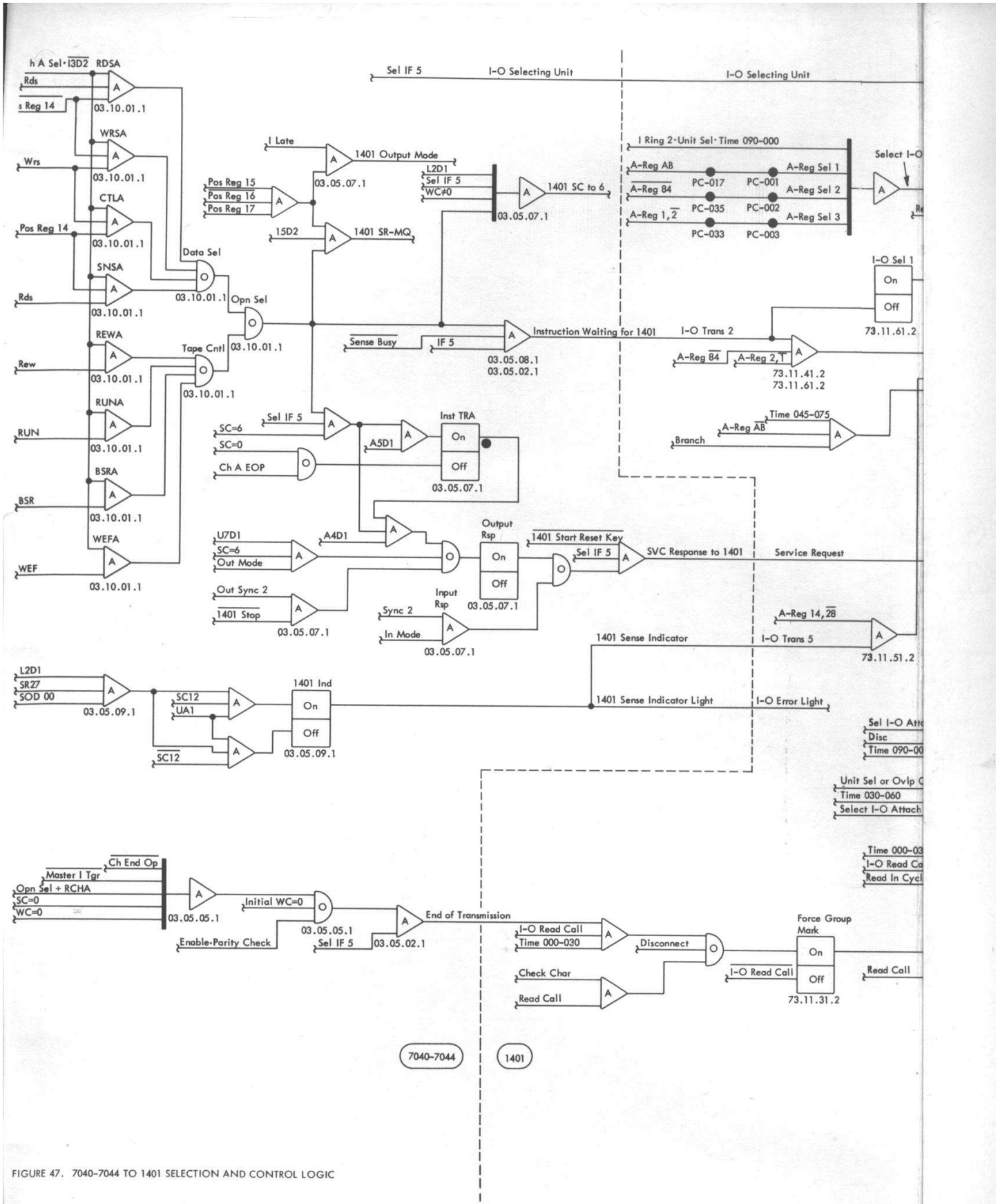
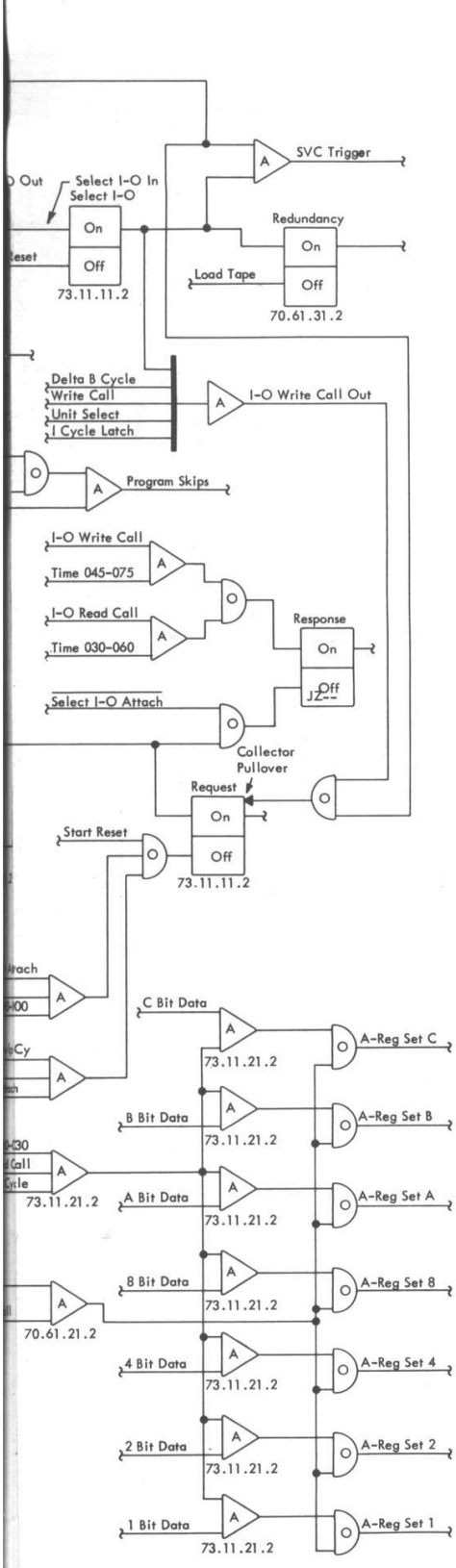


FIGURE 47. 7040-7044 TO 1401 SELECTION AND CONTROL LOGIC



	5	0	1	2	3	4	5	0	1	2	3	4	5	0	
1. I Early							A5								02.15.31.1 01D3COBG
2. I Late			1·A2							A2					02.15.30.1 01D3B14F
3. Unit Address 1				I3D2											03.05.09.1
4. SOD 00				ISB-SR											03.05.09.1
5. SR 27				ISB-SR											03.05.09.1
6. 1401 Indicator Tgr							3·4·5·L2								03.05.09.1
7. 1401 Sense Indicator							6								03.05.02.1

FIGURE 48. SLNA INSTRUCTION INITIAL TIMING

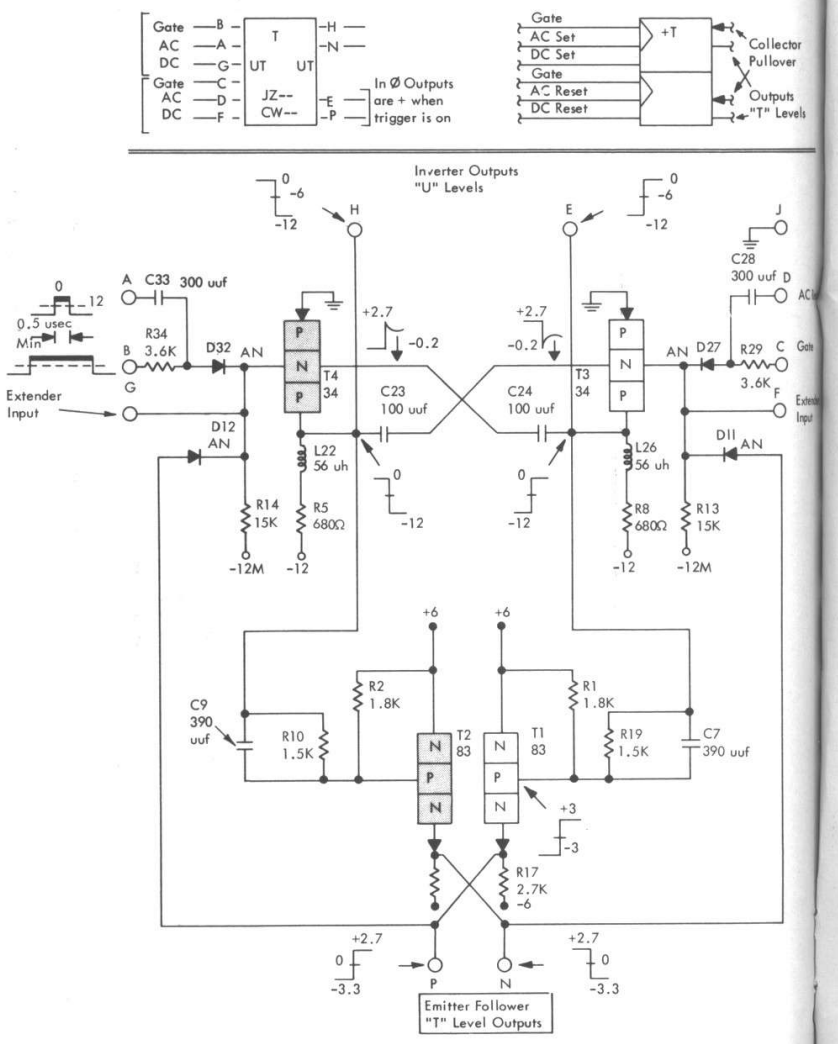


FIGURE 49. JZ--371082; CW--371534 TRIGGERS

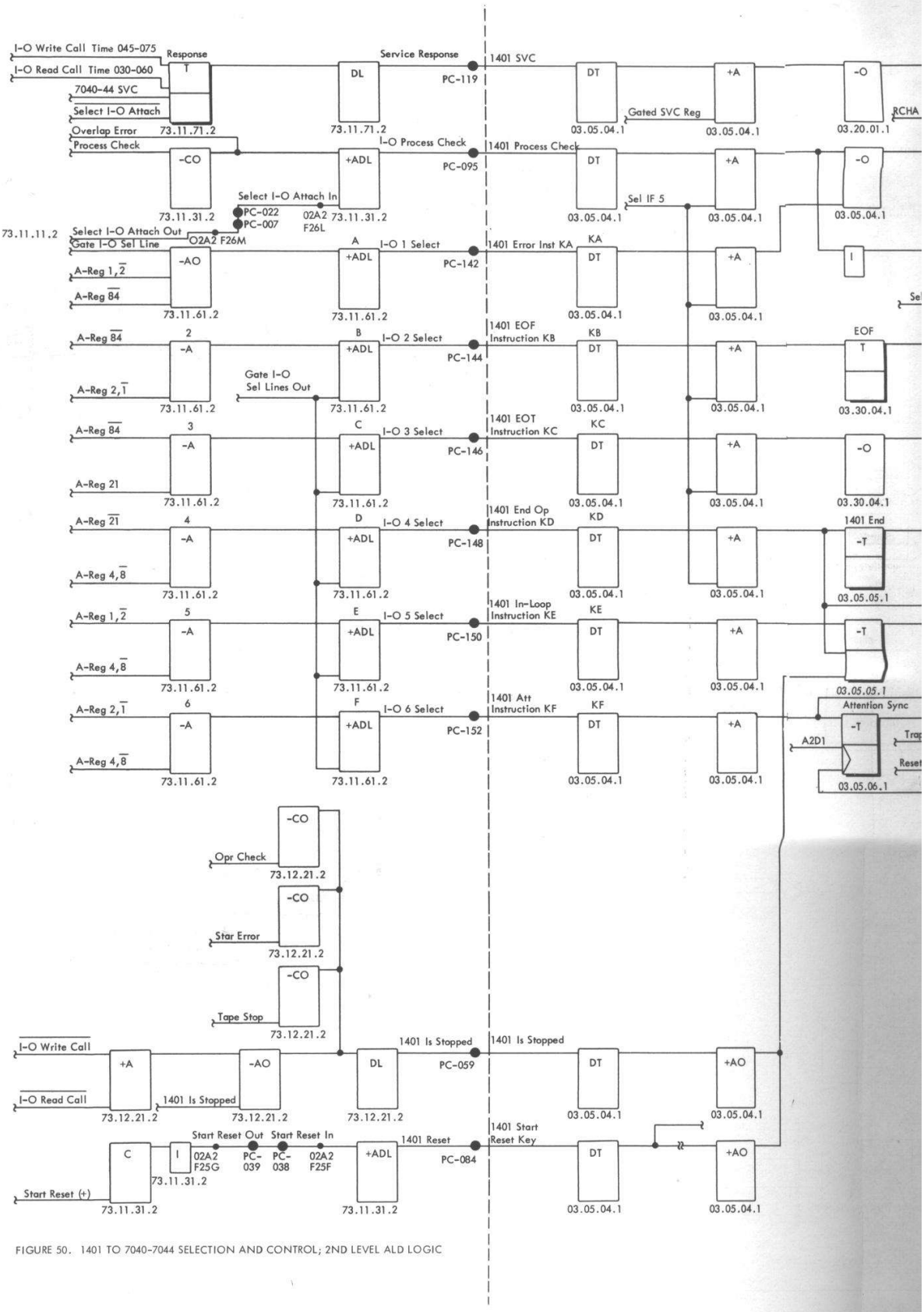
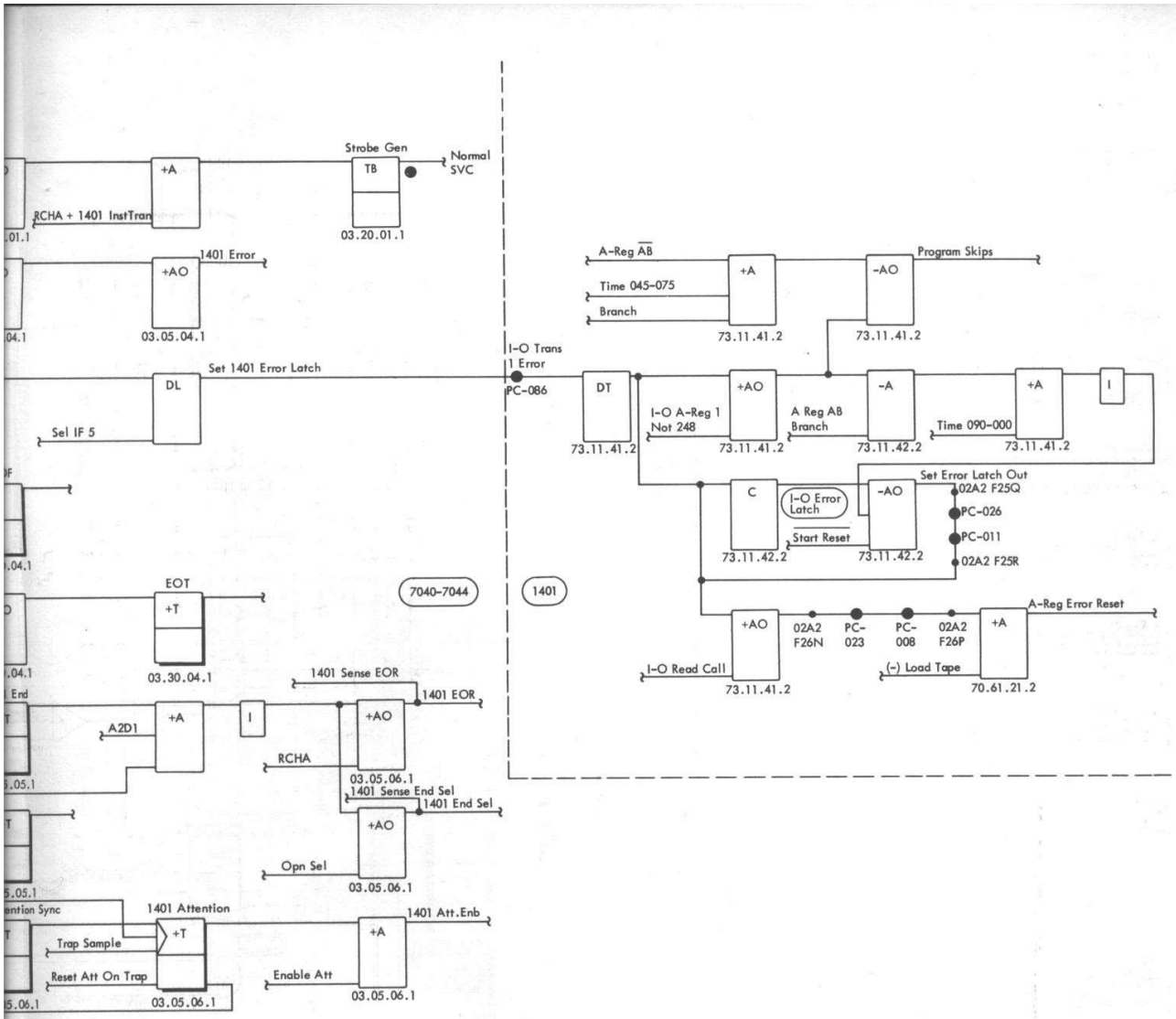


FIGURE 50. 1401 TO 7040-7044 SELECTION AND CONTROL; 2ND LEVEL ALD LOGIC


Strobe Gen
Normal SVC
+A
TB
RCHA + 1401 InstTran
03.20.01.1
1401 Error
+AO
03.05.04.1
A-Reg AB
Time 045-075
Branch
+A
73.11.41.2
-AO
Program Skips
73.11.41.2
I-O Trans 1 Error
PC-086
Set 1401 Error Latch
DL
Sel IF 5
DT
73.11.41.2
I-O A-Reg 1 Not 248
+AO
73.11.41.2
A Reg AB Branch
-A
73.11.42.2
Time 090-000
+A
73.11.41.2
1
Set Error Latch Out
02A2 F25Q
PC-026
PC-011
02A2 F25R
C
I-O Error Latch
Start Reset
-AO
73.11.42.2
73.11.42.2
7040-7044
1401
EOT
+T
03.30.04.1
A-Reg Error Reset
+AO
02A2 F26N
PC-023
PC-008
02A2 F26P
+A
I-O Read Call
73.11.41.2
(-) Load Tape
70.61.21.2
1401 Sense EOR
1401 EOR
A2D1
+A
1
+AO
RCHA
03.05.06.1
1401 Sense End Sel
1401 End Sel
+AO
Opn Sel
03.05.06.1
1401 Attention
+T
Trap Sample
Reset Att On Trap
03.05.06.1
1401 Att.Enb
+A
Enable Att
03.05.06.1

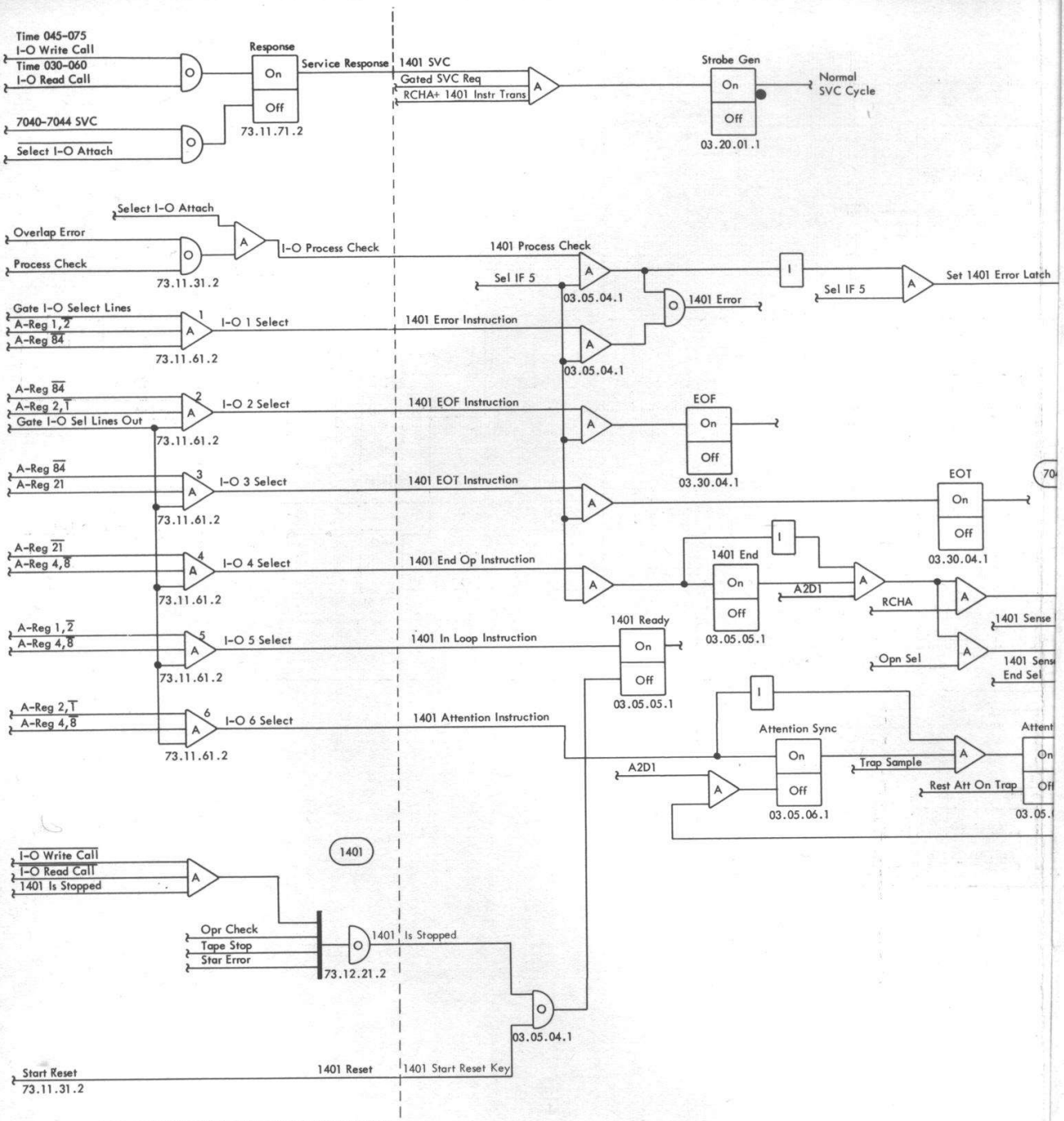


FIGURE 51. 1401 TO 7040-7044 SELECTION AND CONTROL LOGIC

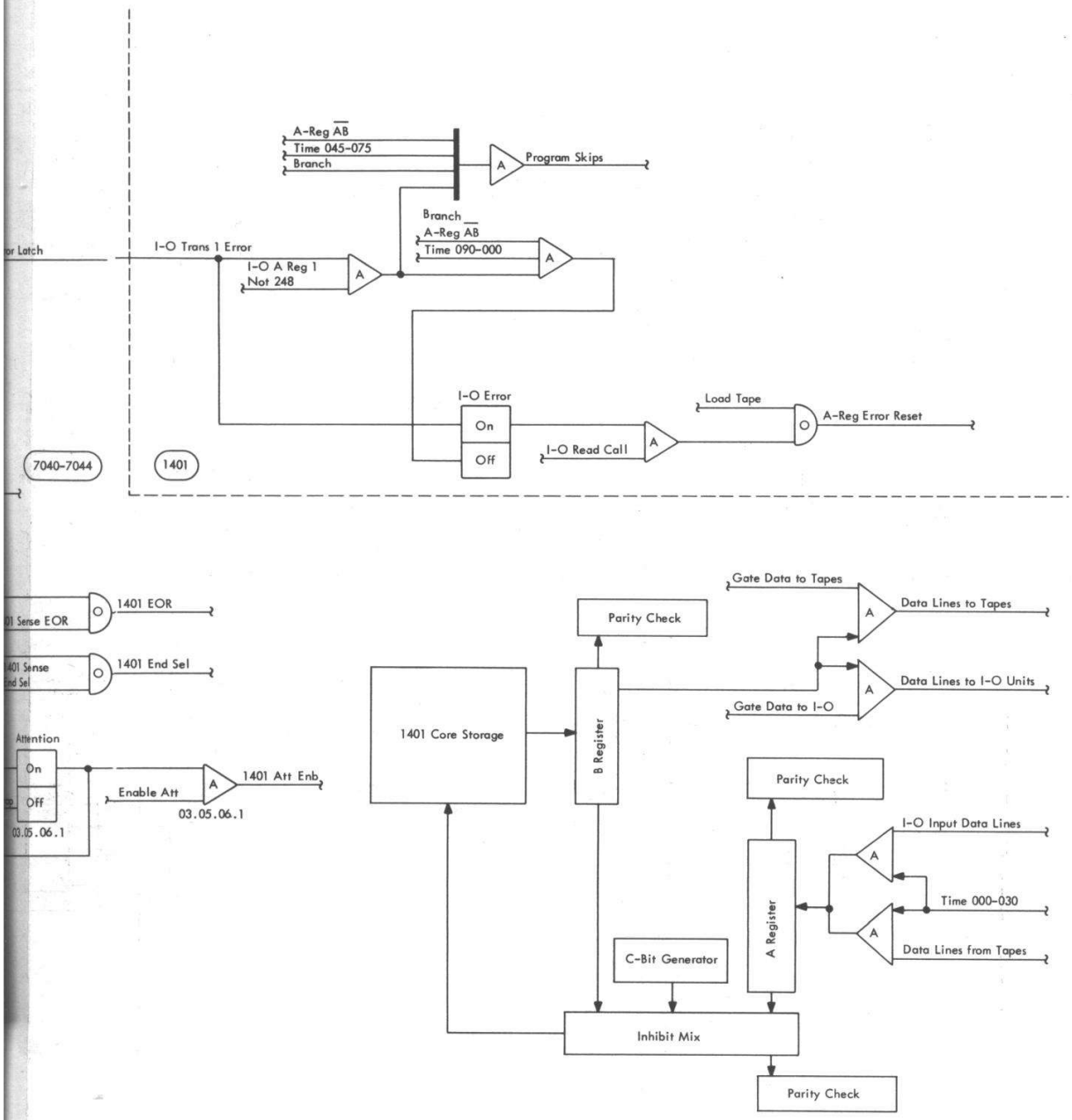


FIGURE 52. BLOCK LOGIC SERIAL I-O ADAPTER

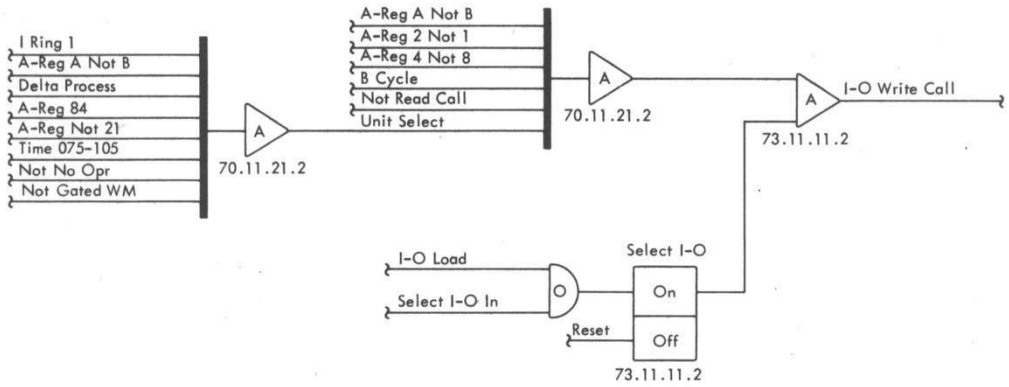


FIGURE 53. 1401 I-O WRITE CALL