

ORIGINAL A FIELD "863" WM AB2 C62 21
 OR ORIGINAL B FIELD "7C3" WM 421 CAB21 21

SIGNAL NAME	FRAME GATE CH	TEST POINT	LOGIC	CYCLE																																			
				T	A	B	A	B	A	B	T	OP	T	A	B	T	OP																						
				3	6	9	0	3	6	9	0	3	6	9	0	3	6	9	0	3	6	9	0	3	6	9	0	3	6	9	0	3	6	9	0	3	6	9	0
1 STORAGE ADDRESS REGISTER			32.35.XX 32.36.XX	[Timing diagram for STORAGE ADDRESS REGISTER]																																			
2 B-REGISTER			35.11.XX	[Timing diagram for B-REGISTER]																																			
3 A-REGISTER			35.16.XX	[Timing diagram for A-REGISTER]																																			
4 +U COMPARE OPERATION	01B1		35.24.11	[Timing diagram for COMPARE OPERATION]																																			
5 -T GATED WORD MARK	01B2		31.07.11	[Timing diagram for GATED WORD MARK]																																			
6 -T I/E CHANGE	01B2		31.05.31	[Timing diagram for I/E CHANGE]																																			
7 +U DELTA T CYCLE	01B2		31.21.11	[Timing diagram for DELTA T CYCLE]																																			
8 -T T CYCLE	01B2		31.24.11	[Timing diagram for T CYCLE]																																			
9 +U T STAR RESTORE	01A8		32.39.11	[Timing diagram for T STAR RESTORE]																																			
10 -T DELTA A CYCLE	01B2		31.22.11	[Timing diagram for DELTA A CYCLE]																																			
11 -T A CYCLE	01B2		31.25.11	[Timing diagram for A CYCLE]																																			
12 -T DELTA B CYCLE	01B2		31.23.11	[Timing diagram for DELTA B CYCLE]																																			
13 +U B CYCLE	01B2		31.26.11	[Timing diagram for B CYCLE]																																			
14 +U TRANSFER B REGISTER	01A3		35.18.11	[Timing diagram for TRANSFER B REGISTER]																																			
15 +U I/E CONTROL 1	01B2		31.05.21	[Timing diagram for I/E CONTROL 1]																																			
16 -T B REG ZONE INHIBIT	01B4		36.13.21	[Timing diagram for B REG ZONE INHIBIT]																																			
17 -T B REG DIGIT INHIBIT	01B4		36.13.21	[Timing diagram for B REG DIGIT INHIBIT]																																			
18 -T B REG C BIT INHIBIT	01A3		35.18.21	[Timing diagram for B REG C BIT INHIBIT]																																			
19 -T B REG WM INHIBIT	01A3		35.40.21	[Timing diagram for B REG WM INHIBIT]																																			
20 +U COMPARE EQ LATCH OUTPUT	01B6		34.21.21	[Timing diagram for COMPARE EQ LATCH OUTPUT]																																			
21 -T EQUAL CHARACTER	01B6		34.21.11	[Timing diagram for EQUAL CHARACTER]																																			
22 -T COMPARE UNEQUAL LAT OUTPUT	01B6		34.21.21	[Timing diagram for COMPARE UNEQUAL LAT OUTPUT]																																			
23 +U HIGH LATCH	02A8		44.34.21	[Timing diagram for HIGH LATCH]																																			
24 +U A REG WM LATCH	01B2		31.06.11	[Timing diagram for A REG WM LATCH]																																			
25 -T MODIFIER CONTROL - 1	01A8		32.42.21	[Timing diagram for MODIFIER CONTROL - 1]																																			
26 -T MODIFIER CONTROL TRANSFER	01A8		32.42.41	[Timing diagram for MODIFIER CONTROL TRANSFER]																																			