



Card Code	Part No 37----	Cplg N'work		Circuit Used as		Input Levels		In $\emptyset$ Output		Out $\emptyset$ Output		Ma. Output		usec Delay per				
		In $\emptyset$	Out $\emptyset$			Min.	Max.	Min.	Max.	Min.	Max.	In $\emptyset$	Out $\emptyset$	Block	100uu Load	Driven Base		
AAZW	1204	Yes	Yes	+A	-O	+0.4	See driver for max Output Levels	-5.6	-3.5	-5.6	-3.0							
AAZV	1205	Yes	No	+AO	-OA	-0.4		-6.4	-6.4				Min.	4.82	5.31	.03	.02	.03
AAZU	1206	No	Yes	+TA	-TO			-7.1	-7.1				Nom	6.0	7.6	.06	.025	.035
AA--	1207	No	No										Max	7.3	10.2*	.1	.03	.04

\*Plus the number of inputs times .044ma

**Current Mode Two-Way AND**

The two-way N type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of two +N inputs produces a +P in-phase output and a -P out-of-phase output.

**Circuit Description**

This circuit uses two transistors (T5 and T6) in an AND configuration similar to diode circuitry (the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive, 6v, supply). The emitter output of this AND circuit drives into a grounded base amplifier T4 referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v any -N input will pull the emitter line

below ground and reverse-bias T4 as shown. In this state, output B is at a -P level of -6.8v because of divider current through its coupling network, and output A is at a +P level of -4.4v because of current flow (7.6ma) out of its coupling network through T5 and T6 to +6v.

When all inputs are positive, the emitter of T4 attempts to rise above ground. In so doing, it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so output A falls to a -P level and output B rises to a +P level because T4 is on.

**Application**

For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases, cap codes zu, zv, and zw -- are used as required (see chart). This circuit is also combined with an OR circuit to make up a trigger and with other AND circuit blocks to obtain DOT functions. DOT functions are obtained by connecting similar output pins together to share a common collector load.