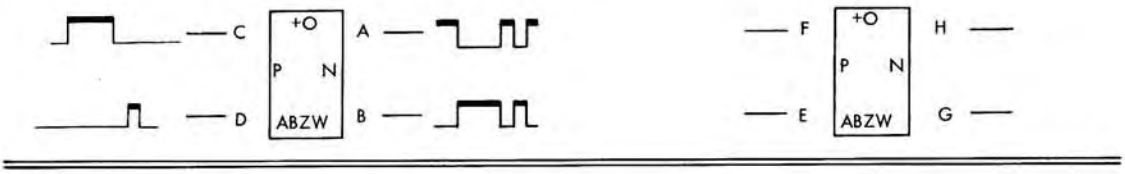

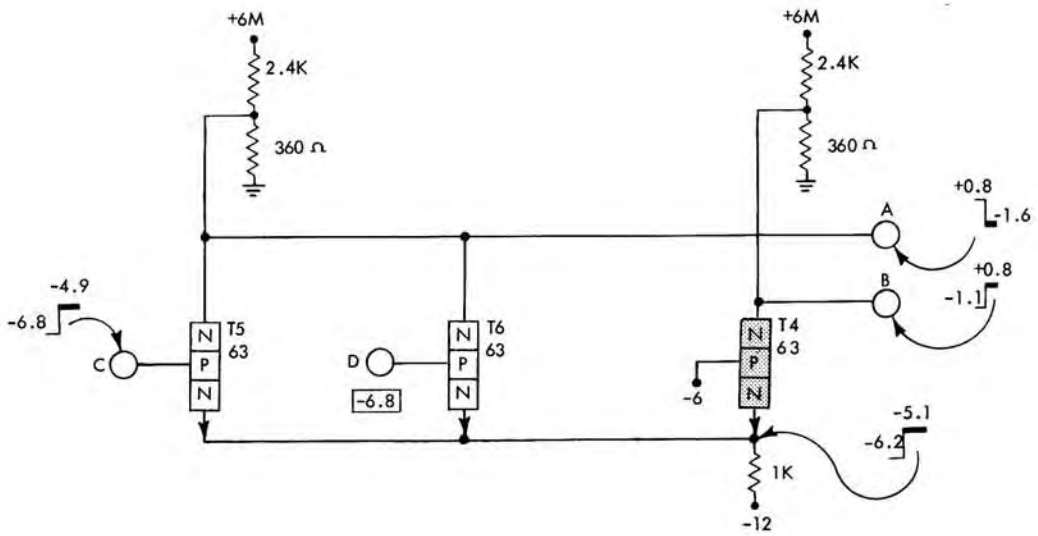

Card Code	Part No 37---	Cplg N'work Out Ø	Cplg N'work In Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.
ABZW	1213	Yes	Yes	+O	-A	-5.6	See driver for max. Output Level	+0.4	+1.2	+0.4	+1.2
ABZV	1214	Yes	No	+OA	- AO	-6.4		-0.4	-2.5	-0.4	-3.0
ABZU	1215	No	Yes	+TO	-TA						
AB--	1216	No	No								

	Ma. Output In Ø	Ma. Output Out Ø	usec Delay per Block	usec Delay per 100uu Load	usec Delay per Driven Base
Min.	4.82	5.31	.03	.02	.03
Nom.	6.0	7.6	.06	.025	.035
Max.	7.3	10.2*	.1	.03	.04

*Plus the number of inputs times .044ma

Current Mode Two-Way OR

The two-way P type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output.

Circuit Description

This circuit uses two transistors (T5 and T6) in an OR configuration similar to diode circuitry; i.e. the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (−12v). The emitter output of this OR circuit drives into a grounded base amplifier T4 referenced to −6v. In this state, all inputs are −P as shown, and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −1.1v because of current flow (6ma) through T4 into its coupling network. Output A is at a +N level of +0.8v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and T4 is reverse-biased and cuts off. Output B rises to a +N level because of divider current through its coupling network, and output A falls to a −N level of −1.6v because of current flow (7.6ma) through an input transistor into its coupling network.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases cap codes ZT - -, ZU and ZV are used as required (see chart). This circuit is also combined with an AND circuit to make up a trigger with other OR circuit blocks to obtain DOT functions. DOT functions are obtained by connecting similar output pins together to share a common collector load.