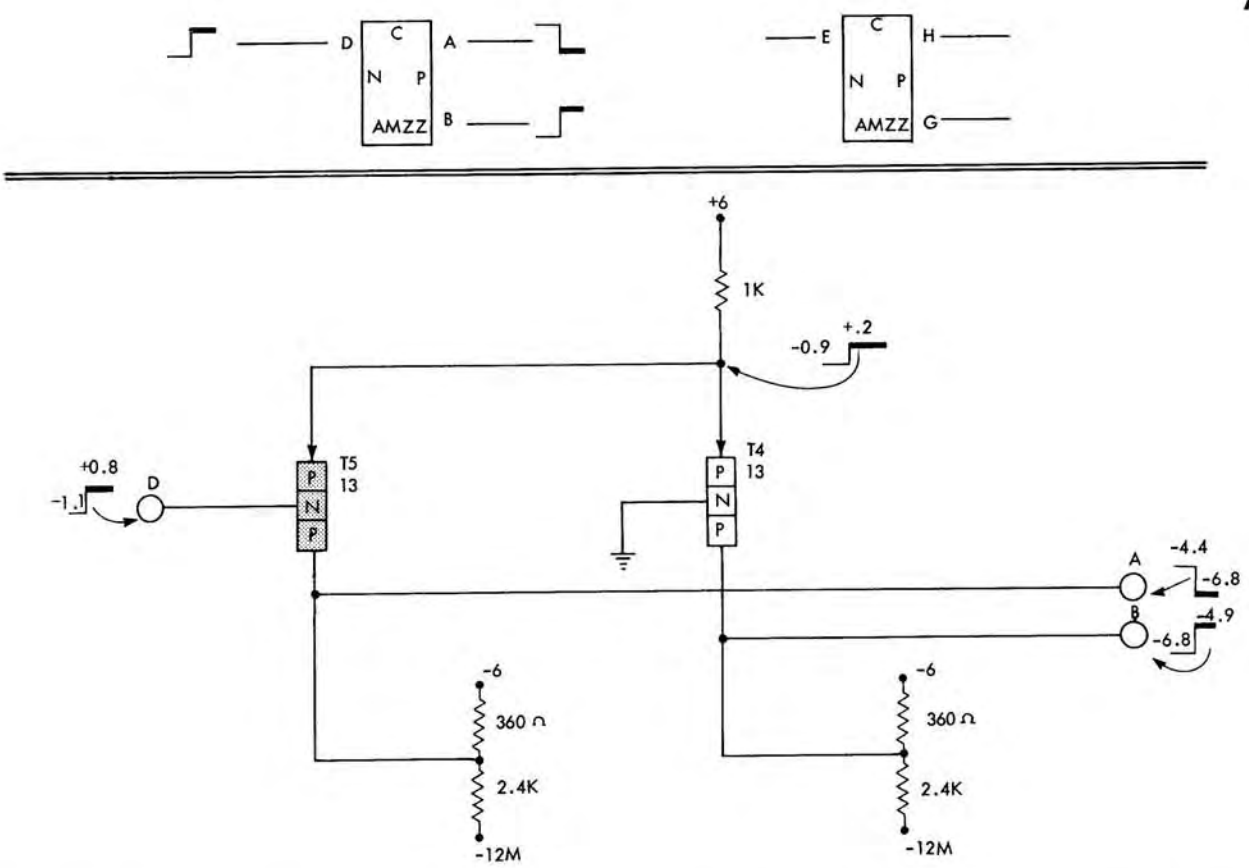


| Card Code | Part No. 37---- | Cplg Network In Ø | Cplg Network Out Ø | Circuit Used as | | Input Levels Min. | Input Levels Max. | In Ø Output Min. | In Ø Output Max. | Out Ø Output Min. | Out Ø Output Max. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AMZZ | 1200 | Yes | Yes | C | CO | +0.4 | See driver for max. Output Levels | -5.6 | -3.5 | -5.6 | -3.0 |
| AMZY | 1201 | Yes | No | TC | | | | | | | |
| AMZX | 1202 | No | Yes | | | -0.4 | | -6.4 | -7.1 | -6.4 | -7.1 |
| AM-- | 1203 | No | No | | | | | | | | |

| | Ma Input In Ø | Ma Input Out Ø | usec Delay per Block | usec Delay per 100 uu Load | usec Delay per Driven Base |
|---|---|---|---|---|---|
| Min. | 4.82 | 5.31 | .03 | .02 | .03 |
| Nom. | 6.0 | 7.6 | .06 | .025 | .035 |
| Max. | 7.3 | 10.2 | .1 | .03 | .04 |

### Current Mode N-to-P Converter

The N-to-P converter is a single input logic block. It is fed by an N line and produces both an in-phase and out-of-phase output. For a −N line input, a −P in-phase output and a +P out-of-phase output result. It is used:

1. To translate from an N to a P line.
2. To obtain a P line inversion of the input sign, i.e., a +N to a −P or a −N to a +P.
3. As a current amplifier to drive other logic blocks.

*Circuit Description*

This circuit configuration is that of a one-way AND circuit (the input transistor T5 has its base-to-emitter NP diode returned to a positive supply). Its emitter output drives into a grounded base amplifier T4 referenced to ground. T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse-bias T4 as shown. In this state, output B is at a −P level of −6.8v because of divider current through its coupling network, and output A is at a +P level of −4.4v due to current flow (7.6ma) out of its coupling network through T5 to +6v.

When the input to T5 rises to a +N level the emitter of T4 attempts to rise above ground. In so doing it becomes forward-biased and clamps to its base potential. In this state, output B rises to a +P level because of current flow (6ma) out of its coupling network through T4 to +6v and output A falls to a −P level because of divider current through its coupling network.

*Application*

For some applications, the circuit driven by this logic block requires a coupling network other than the 360 ohm and 2.4K resistors shown. In such cases, cap codes ZX, ZY, and -- are used as required (see chart). This circuit is also used as a converter within a trigger (93) and in DOT functions as a CO.