urrent Mode, 3.2 to 215 Microsecond Universal Single-Shot

he AW - - single shot (ss) card is an RC timing network. he required input for this network is supplied by a ansistor amplifier on the card. The circuit is triggered y a positive input signal. Once triggered, it develops an -phase exponential output waveform as shown. This ard is used with a standard AND and OR block to develop square wave output pulse (see logic application drawg). The width of the output square wave is determined y the AW - - card.

Signal information and flow of this multicard circuit as follows. In the inactive state, AND inputs C and D re up, the input and output of the ss are down, and OR put E is up.

To make the circuit active (start the single-shot) a egative signal to AND input C is required. This negative put drops out the AND circuit and its in-phase output alls. Both inputs to the OR circuit are now negative so t drops out; its in-phase output falls and its out-of-phase utput rises. The OR circuit is the output stage of this ulticard circuit, so at this time the leading edge of the quare wave signals desired are recognized at outputs G nd H. These signals are terminated (single-shot time is nded) when OR input F reaches a +P level. Input F tarted rising as shown when the AND circuit first dropped ut because AND output A developed a positive shift and icked the ss.

OR output G is coupled back to AND input D so the ND circuit is held off for at least the duration of the ingle-shot timing. This arrangement insures that the ingle-shot timing is not affected by input C if input C ises before the single-shot timing is completed. When the ingle-shot signal is ended and input C is again positive, he AND circuit is picked. AND output B holds the OR ircuit picked while AND output A drops out the ss. The ignal decay of AND output A is caused by the ss input ircuitry.

Because the AW - - card is a universal timing card (3.2 o 215 microseconds), it is necessary to do the following o obtain a specific timing:

1. Connect back panel wiring as shown in the chart to obtain a specific timing range.
2. Adjust the 10K potentiometer located on the card for the exact timing desired.

Circuit Description

As shown, input C and D are +N and TX3 is forward-biased. Current flow out of the 360 ohm, 2.4K coupling network through TX3 to +6v establishes AND output B at a +P level of −4.9v which forward-biases TX5. Current flow from −12v through TX5 into its coupling network establishes OR output H at a −N level of −1.4v. OR output G is at a +N level of +0.8v because of divider current through its coupling network. Input current to ss input B is zero so the base of T1 is at −12v and T1 is forward-biased. Current flows from −12v through T1, the 4.99K resistor, and the 10K potentiometer to +6v. The emitter of T1 clamps to its base potential and the .0015μfd capacitor develops a 17.8v charge.

When input C falls, TX1 is forward biased and TX3 is cut off. AND output B falls to a −P level of −6.8v which forward biases TX6 and cuts off TX5. With TX5 cut off and TX6 conducting, output H rises to a +N level and output G falls to a −N level. Output G is coupled back to AND input D so TX2 is forward-biased with TX1. Current for TX1 and TX2 flows from −12v through the 2.4K resistor, TX1, and TX2 to +6v. When the voltage drop across the 2.4K resistor is greater than 6v, D1 is forward-biased, current flows from −6v through D1, TX1 and TX2 to +6v, and the base of T1 reaches a −4v level. T1 is reverse-biased and the .0015μfd capacitor starts to discharge through the 4.99K resistor and 10K potentiometer. If input C were of shorter duration than the single-shot timing, TX1 would cut off. Tx3 is held cut off at this time by TX2 so the rise of input C has no effect.

When the base of TX4 rises above −6v, TX4 is forward-biased and TX6 is cut off. Output G rises to a +N level and output H falls to a −N level. The rising signal to input D forward-biases TX3 and reverse-biases TX2. Current flow through TX3 causes output B to rise and forward bias TX5 and cut off TX6. With TX2 cut off, T1 is again forward-biased and T1 supplies input current to the .0015μfd. capacitor to again charge it to 17.8v.

Had input C been of greater duration than output G, TX2 would have cut off when output G rose, but TX3 would be held off by TX1.

The amount of capacitance wired to ss output H determines the timing range (from and to timing) of the ss. A specific time within the range is obtained by adjusting the 10K potentiometer located on card AW - -.