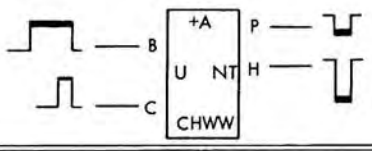

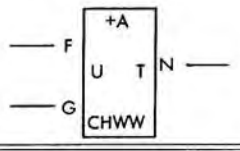

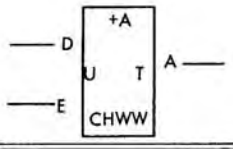

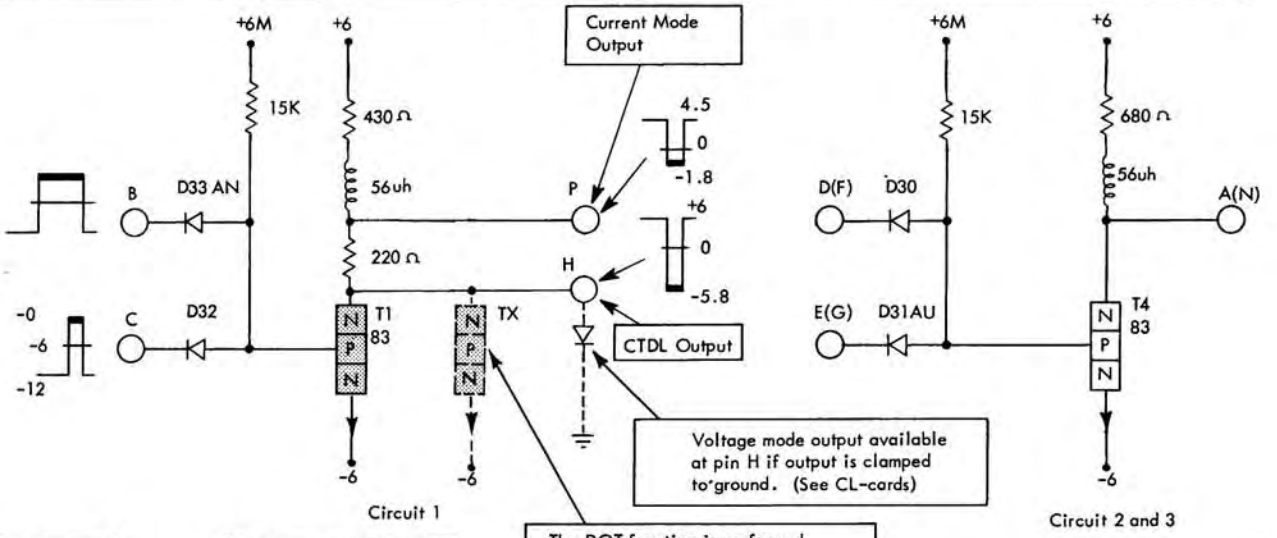

Input Levels	
Min.	Max.
-5.3 to -7.4	0.24 to -12.48

Output Levels			
Current Mode		CTDL	
Min.	Max.	Min.	Max.
+2.8 to -1.1	6.3 to -2.5	1.44 to -5.5	6.3 to -6.3

Card Code	Part No 37----	E'tender Input Circuit	CM Output Circuit	Collector Loading Ckt 1	Ckt 2	Ckt 3	Delays Per		Basic Block	Par'lel C'ltor	CM Base	Diode Input	100 uufd	Circuit Use	
CHWW	1252	No	1	Yes	Yes	Yes	Turn On	Min.	.18	.00	.00	.00	.02	+A	-O
CHVW	1264	No	1	Yes	Yes	No		Max.	.52	.007	.02	.02	.05	+AO	-AO
CHVV	1265	No	1	Yes	No	No	Turn Off	Min.	.05	.004	.005	.000	.03	+CO	-CA
CH--	1266	No	No	No	No	No		Max.	.12	.01	.02	.005	.06	+C	+TC
														+TCO	+TAO

CTDL Two-Way +AND

The CHWW card consists of three two-way NPN logic circuits. Each circuit on the card normally performs a +AND and INVERT logical function that translates a U input to an out-of-phase T output. All three circuits on the card have internal collector loads that provide CTDL outputs at pins H, A, and N and a suitable current-mode output at pin P.

Circuit Description (Circuit 1)

The +AND function is performed by the diode switch of D33 and D32 returned to +6v, and the INVERT function is accomplished by the transistor circuit. Coincidence of +U levels is required at input pins B and C to forward-bias T1 into saturation. With T1 on, the output at pin H nears −6v (minus the small voltage drop across the transistor). When either of the input signals drops to −12v, T1 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region and minimizes the effect of operating the transistor in saturation. This action assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance, and the output at pin H increases toward +6v (No Load). The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current mode output.

Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL, current-mode, and voltage-mode outputs are available from these circuits as noted on the schematic.