



Input Level	
Min	Max
+1.44	6.24
-0.74	-6.24

Output Levels			
Current Mode		CTDL	
Min	Max	Min	Max
-4.9	-3.5	-0.54	+0.24
-8.8	-12.48	-7.44	-12.48

Card Code	Part No 37----	Extender Inputs	CM Output	Collector Loading		Delays (usec)					Circuit Use		
				Circuit	Ckt 1	Ckt 2	Turn On	Min.	Basic Block	Parallel Collector	CM Base	Diode Input	100 uufd
CJWV	1253	1	1	Yes	Yes	Min.	0.20	0.00	0.00	0.00	0.02	+O	-A
						Max.	0.70	0.007	0.015	0.02	0.05	+OA	-AO
CJVU	1267	1	1	Yes	No	Min.	0.06	0.004	0.005	0.00	0.03	+CA	-CO
						Max.	0.18	0.01	0.02	0.005	0.06	-TA	-TC
CJ--	1268	1	No	No	No							-TCO	+C

CTDL Three-Way —AND

The cjwv card consists of two three-way PNP logic circuits. Each circuit on the card normally performs a -AND and INVERT logical function and translates a T input to an out-of-phase U output. Both circuits on the card have internal collector loads that provide CTDL outputs at pins N and H and a suitable current-mode output at pin P. Extender pin G permits additional inputs to control circuit 1.

Circuit Description (Circuit 1)

The -AND function is performed by the diode mix of D33, D31 and D32 returned to -12v, and the INVERT function is accomplished by the transistor circuit. Coincidence of -T levels is required at input pins D, E, and F to forward-bias T2 into saturation. With T2 on, the output at pin N nears 0v (minus the small voltage drop across the transistor). When either of the input signals increases to +6v, T2 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region and minimizes the effect of operating the transistor in saturation. This action

assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin N decreases to -12v (No Load). The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current-mode output.

Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL, current-mode, and voltage-mode outputs are available from these circuits as noted on the schematic.