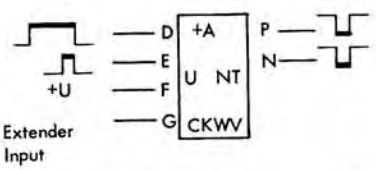

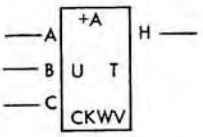

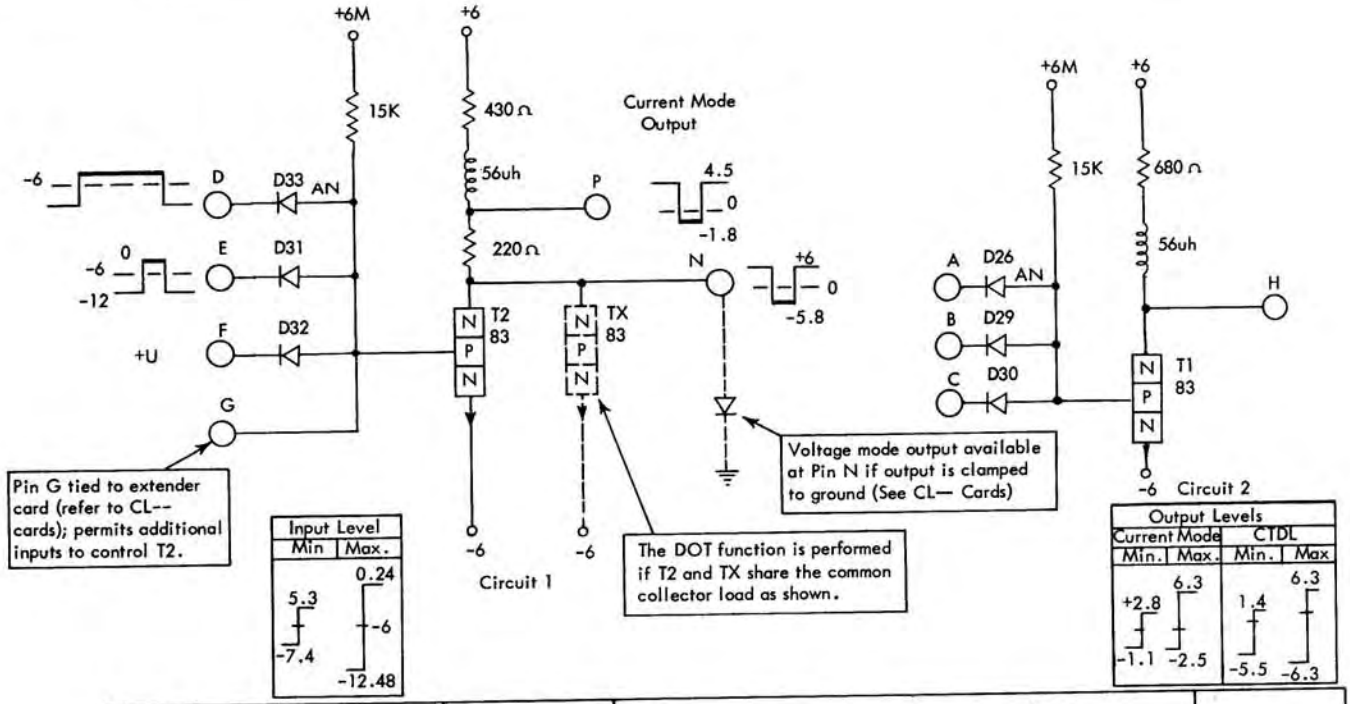

Card Code	Part No 37----	Extender Input	CM Output	Collector Loading Circuit		Delays	Per	Basic Block	Par'lel Collector	CM Base	Diode Input	100 uufd	Circuit Use	
		Circuit	Circuit	1	2									
CKWV	1254	1	1	Yes	Yes	Turn On	Min.	.18	.00	.00	.00	.02	+A	-O
							Max.	.52	.007	.02	.02	.05	+AO	-OA
CKVU	1269	1	1	Yes	No	Turn Off	Min.	.05	.004	.005	.000	.03	+CA	+C
CK--	1270	1	No	No	No		Max.	.12	.01	.02	.005	.06	+TAO	-TCO
													+TA	+TC

(usec)

CTDL Three-Way +AND

The CKWV card consists of two three-way NPN logic circuits. Each circuit on the card normally performs a +AND and INVERT logical function and translates a U input to an out-of-phase T output. Both circuits on the card have internal collector loads that provide CTDL outputs at pins N and H and a suitable current-mode output at pin P. Extender pin G permits additional inputs to control circuit 1.

Circuit Description (Circuit 1)

The +AND function is performed by the diode switch of D33, D31, and D32 returned to +6v, and the INVERT function is accomplished by the transistor circuit. Coincidence of +U levels is required at input pins D, E, and F to forward-bias T2 into saturation. With T2 on, the output at pin N nears −6v (minus the small voltage drop across the transistor). When either of the input signals drops to −12v, T2 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a faster response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin N increases to +6v (No Load). The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current-mode output.

Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading conditions for the different cap connections in this group of cards are noted above. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL, current-mode, and voltage-mode outputs are available from these circuits as noted on the schematic.