



| Card Code | Part No 37--- | Extender Input Circuit | CM Output Circuit | Collector Loading Circuit | | | | Delays (usec) | | | | | | Circuit Use | |
|-----------|---------------|------------------------|-------------------|---------------------------|-----|-----|-----|---------------|-------------|------------------|---------|-------------|----------|-------------|--------------------------------|
| | | | | 1 | 2 | 3 | 4 | Per | Basic Block | Par'lel C'lector | CM Base | Diode Input | 100 uufd | | |
| CRVZ | 1274 | 1,2 | No | Yes | Yes | Yes | Yes | Turn On | Min. | 0.18 | .00 | .00 | .00 | .02 | +C CO +TC +TCO -CA |
| CRZT | 1275 | 1,2 | No | Yes | Yes | No | No | | Max. | 0.52 | .007 | .02 | .02 | .05 | |
| CRYG | 1277 | 1,2 | No | Yes | No | No | No | Turn Off | Min. | 0.05 | .004 | .005 | .000 | .03 | |
| CR-- | 1276 | 1,2 | No | No | No | No | No | | Max. | 0.12 | .01 | .02 | .005 | .06 | |

CTDL U to T Converter

The CRVZ card consists of four one-way NPN logic circuits. Each circuit on the card translates a U input to an out-of-phase T output. Internal collector loading for each circuit gives CTDL outputs at pins G, C, P and A. Extender pins N and B permit additional inputs to control circuits 1 and 2.

A +U level is required at pin E to forward-bias T1 on. With T1 on, the output at pin G is near -6v minus the slight voltage drop across the forward-biased transistor. When the input signal drops to -12v, T1 is turned off. The low forward impedance of the conducting diode rapidly removes the excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin G increases to +6v (No Load).

Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

The circuit loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT function is accomplished by connecting similar output pins together to share a common collector load. CTDL and voltage-mode outputs are available from these circuits as noted on the schematic.