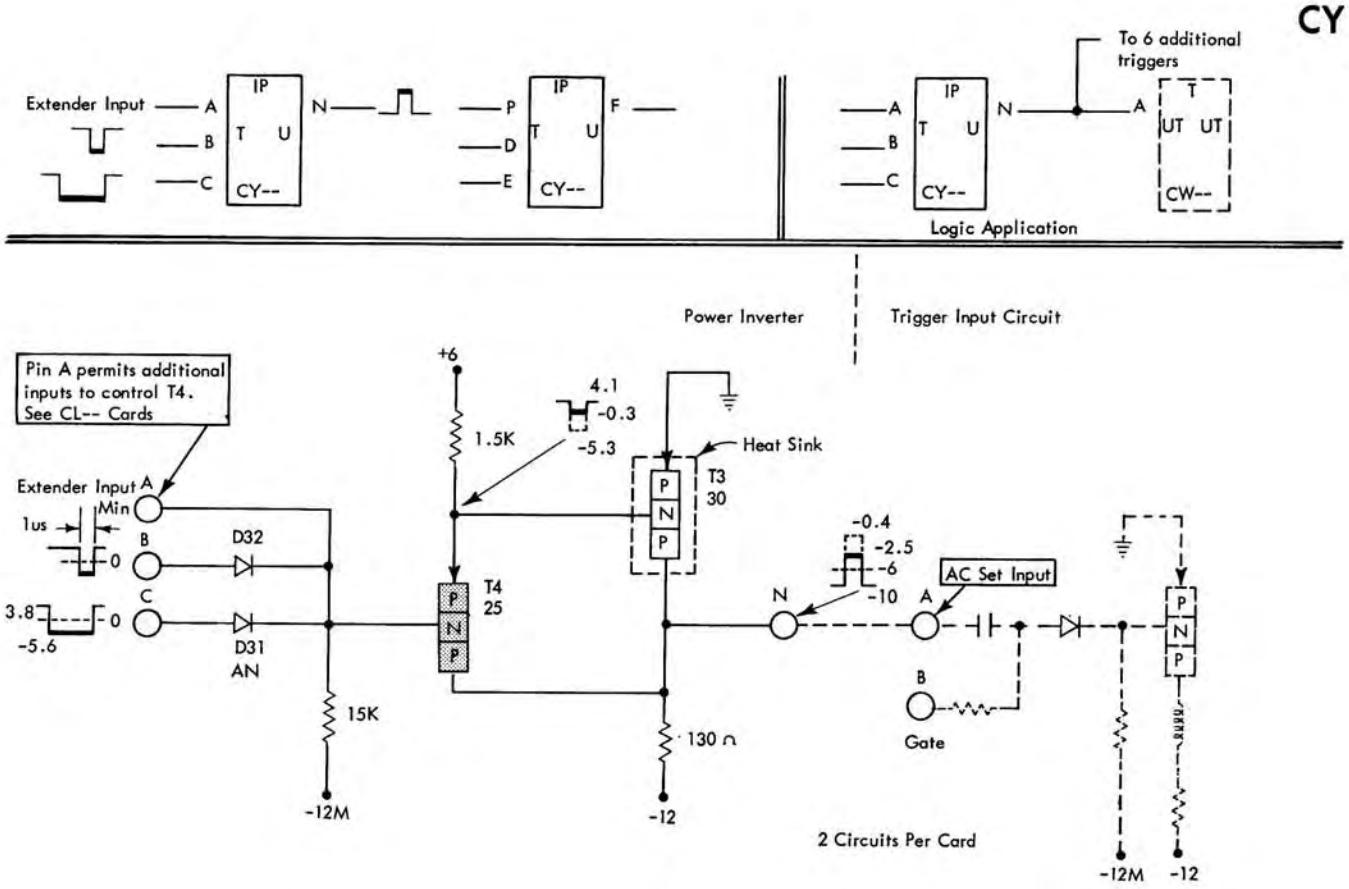

CY--371542

Input Level		Output Levels		Delay		usec
Min.	Max.	Min.	Max.		Per	Circuit
1.44 / -1.14	+6.2 / -6.2	-0.4 / -9.	+0.2 / -12.48	Turn On	Min.	0.21
					Max.	0.60
				Turn Off	Min.	0.24
					Max.	0.37

CTDL Power Inverter

The CY - - card consists of two power inverter circuits used to drive the AC set inputs of the CTDL triggers or equivalent loading. Each circuit is basically a modified emitter follower driving an inverter. Relatively small input signals develop a large power output capable of driving seven CTDL triggers or a maximum capacitive load of 1650$\mu\mu$fd. The input arrangement is similar to the CTDL logic block, and has two diode inputs and an extender input. A −T line of at least one microsecond duration at all inputs is required to drive T4 into maximum conduction.

Circuit Description

If any of the inputs at pins A, B, or C are up (3.8v), minimum current flows in the emitter follower T4 and the 1.5K resistor. The emitter follower output (4.1v) reverse-biases T3 off. Minimum current flow from the −12v supply, 130 ohm resistor to the emitter follower circuit sets the output at pin N to near −10v.

When all inputs at pins C, B, and the extended input are down (−5.6v), maximum current flows through T4. The emitter follower output decreases toward −5.3v, but is clamped at −0.3v when T3 becomes forward-biased and conducts. When T3 turns on, increased current through the 130 ohm resistor quickly raises the output at pin N to −2.5v, and up to 30ma is supplied to the AC set inputs of the CTDL triggers or to equivalent loading.

The 130 ohm resistor relates the two collectors so that if T3 becomes saturated, the current through T4 is decreased, which in turn reduces the base current to T3. This degenerative action prevents T3 from operating in saturation and provides medium current outputs with minimum turn-on and turn-off delays.