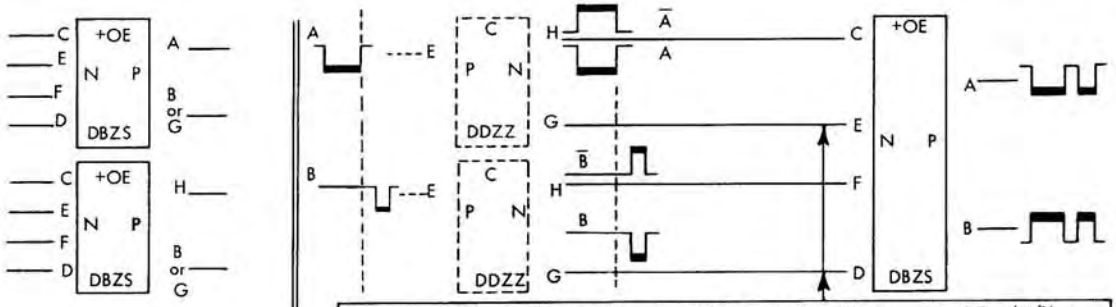


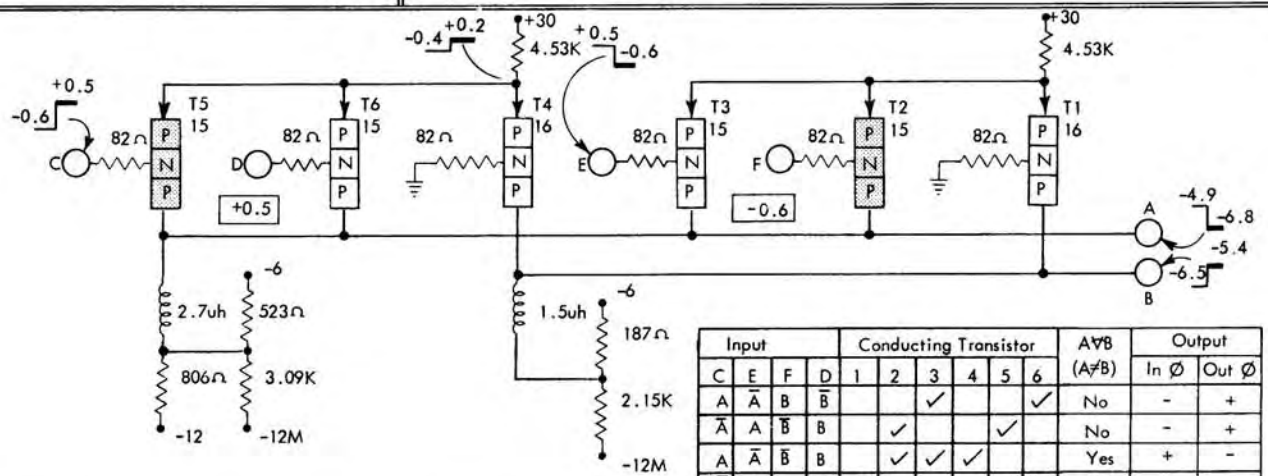


| Input | | | | Conducting Transistor | | | | | | A∀B | Output | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C | E | F | D | 1 | 2 | 3 | 4 | 5 | 6 | (A≠B) | In Ø | Out Ø |
| A | $\bar{A}$ | B | $\bar{B}$ | | | ✓ | | | ✓ | No | - | + |
| $\bar{A}$ | A | $\bar{B}$ | B | | ✓ | | | ✓ | | No | - | + |
| A | $\bar{A}$ | $\bar{B}$ | B | | ✓ | ✓ | ✓ | | | Yes | + | - |
| $\bar{A}$ | A | B | $\bar{B}$ | ✓ | | | | ✓ | ✓ | Yes | + | - |

| Card Code | Part No 37---- | Cplg Network In Ø | Cplg Network Out Ø | Circuit used as | | Input Levels Min. | Input Levels Max. | In-phase Output Min. | In-phase Output Max. | Out-phase Output Min. | Out-phase Output Max. | Ma. Output | In Ø | Out Ø (On) | Out Ø (Off) | musec block delay Turn On | musec block delay Turn Off |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DBZS | 1288 | Yes | Yes | +OE | | +0.4 -0.4 | See driver for max. output levels | -5.6 -6.4 | -5.2 -6.5 | -5.6 -6.4 | -4.2 -7.1 | Min. | 5.97 | 12.07 | 6.04 | 8 | 4 |
| DBZR | 1289 | Yes | No | | | | | | | | | Nom. | 6.59 | 13.40 | 6.75 | 15 | 9 |
| DBZQ | 1290 | No | Yes | | | | | | | | | Max. | 7.20 | 14.72 | 7.45 | 24 | 15 |
| DBZP | 1291 | No | No | | | | | | | | | | | | | | |

## Diffused Junction, Plus Exclusive OR

The +OE circuit is a special type of OR circuit. It develops a +P in-phase output and a −P out-of-phase output when an A∀B (read A exclusive OR B) statement is recognized at the input. This statement simply means A ≠B. In order to clarify what this means, the signal information-flow in the logic application above is described. First, two pieces of information, signals A and B, are passed through converters. These signals and their complements are mixed at the input of the +OE. Of these four inputs, the signals of two (either E and D or C and F) must be compared to establish if A≠B (See the note associated with inputs E and D).

A check of the A and B signals shows that first A = B (the A∀B is not established) and output B is −P. Next A falls and B is still up so that A∀B exists and output B is +P. When A again rises, both A and B are up and output B is again −P. Finally B falls with A up and again A∀B is realized; output B is +P. Simply stated, the in-phase output follows the sign of the function for an A∀B input.

*Circuit Description*

In the state shown T5 and T2 are forward-biased and 13.4ma flows out of the 523 ohm, 806 ohm, 3.09K coupling network; 6.7ma flows through T5 to +30v, and 6.7ma flows through T2 to +30v. This current flow out of the network sets output A at a +P level of −4.9v. Divider current through the 187 ohm, 2.15K network establishes output B at a −P level of −6.5v.

Because a signal and its complement appear at two of the inputs, two signals switch simultaneously. Thus, input C rises, which forward-biases T4 and cuts off T5, while input E falls to forward-bias T3. In this state, 6.7ma flows out of the out-of-phase network through T3 and T2 to +30v. Thus, the current flow out of this network falls from 13.4ma to 6.7ma and output A falls to a −P level of −6.8v. Current out of the 187 ohm, 2.15K network flows through T4 to +30v and output B rises to a +P level of −5.4v.

If the signals to inputs D and F had been switched instead of the signal to C and F, the output levels would have switched as described above, only in this case T1 would conduct instead of T4.