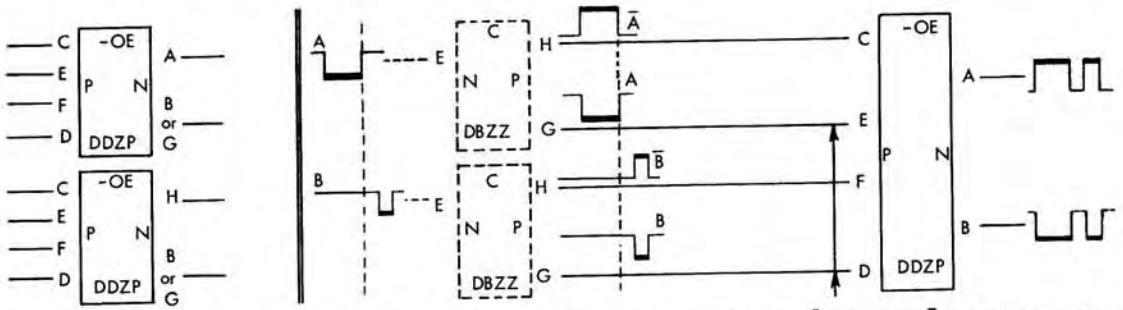

Comparison of the in Ø inputs determines if the exclusive OR statement $[A \forall B = (A \neq B)]$ is established. When established, the in Ø output follows the sign of the function; i.e., the in Ø output is negative for a -OE when $A \neq B$

Input				Conducting Transistor						A∀B	Output	
C	E	F	D	1	2	3	4	5	6	(A≠B)	In Ø	Out Ø
A	Ā	B	B̄		✓			✓		No	+	-
Ā	A	B̄	B			✓			✓	No	+	-
A	Ā	B̄	B	✓				✓	✓	Yes	-	+
Ā	A	B	B̄		✓	✓	✓			Yes	-	+

Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used As		Input Levels Min.	Input Levels Max.	In-phase Output Min.	In-phase Output Max.	Out-phase Output Min.	Out-phase Output Max.
DDZS	1304	Yes	Yes	-OE		-5.6 to -6.4	See driver for max output levels	+0.4 to -0.4	+0.5 to -0.8	+0.4 to -0.4	+1.1 to -1.8
DDZR	1305	Yes	No								
DDZQ	1306	No	Yes								
DDZP	1307	No	No								

Ma Output	In Ø	Out Ø (on)	Out Ø (off)	musec Block Delay Turn On	Turn Off
Min.	5.97	12.07	6.04	7	5
Nom.	6.59	13.40	6.75	15	10
Max.	7.20	14.72	7.45	26	16

Diffused Junction, Minus Exclusive OR

The -OE circuit is a special type of OR circuit. It develops a -N in-phase output and a +N out-of-phase output when an A∀B (read A exclusive OR B) statement is recognized at the input. This statement simply means $A \neq B$. To clarify what this means, the signal information flow in the logic application above is described. First, two pieces of information, signals A and B, are passed through converters. These signals and their complements are mixed at the input of the -OE. Of these four inputs, the signals of two (either E and D or C and F) must be compared to establish if $A \neq B$. (See note, inputs E and D).

A check of the A and B signals shows that first A=B (A∀B is not established) and output B is +N. Next A falls and B is still up, so A∀B exists and output B is -N. When A again rises, both A and B are up and output B is again +N. Finally, B falls with A up and again A∀B is realized; output B is -N. Simply stated, the in-phase output follows the sign of the function for an A∀B input.

Circuit Description

In the state shown, T6 and T3 are forward-biased. A current of 6.7ma flows from -36v through T6 into the 523 ohm, 806 ohm, 3.09K coupling network, and a similar current flows through T3. Thus, a combined current of 13.4ma flows into the coupling network, which establishes output A at a -N level of -1.1v. Divider current through the 187 ohm, 2.15K network establishes output B at a +N level of +0.5v.

Because a signal and its complement appear at two of the inputs, two signals switch simultaneously. Thus, input C rises and forward-biases T5 while E falls and forward-biases T1 and cuts off T3. In this state, 6.7ma flows from -36v through T5 and T6 into the coupling network. Thus, the current flow into the out-of-phase network falls from 13.4ma to 6.7ma and output A rises to a +N level of +0.8v. Current flow from -36v through T1 into the 187 ohm, 2.15K network causes output B to fall to a -N level.

If the signal to inputs D and F had been switched instead of the signal to C and F, the output levels would have switched as described above, only in this case, T4 would conduct instead of T1.