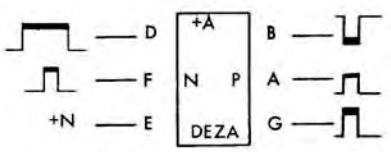

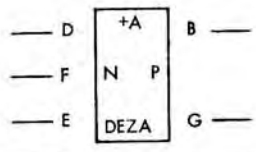

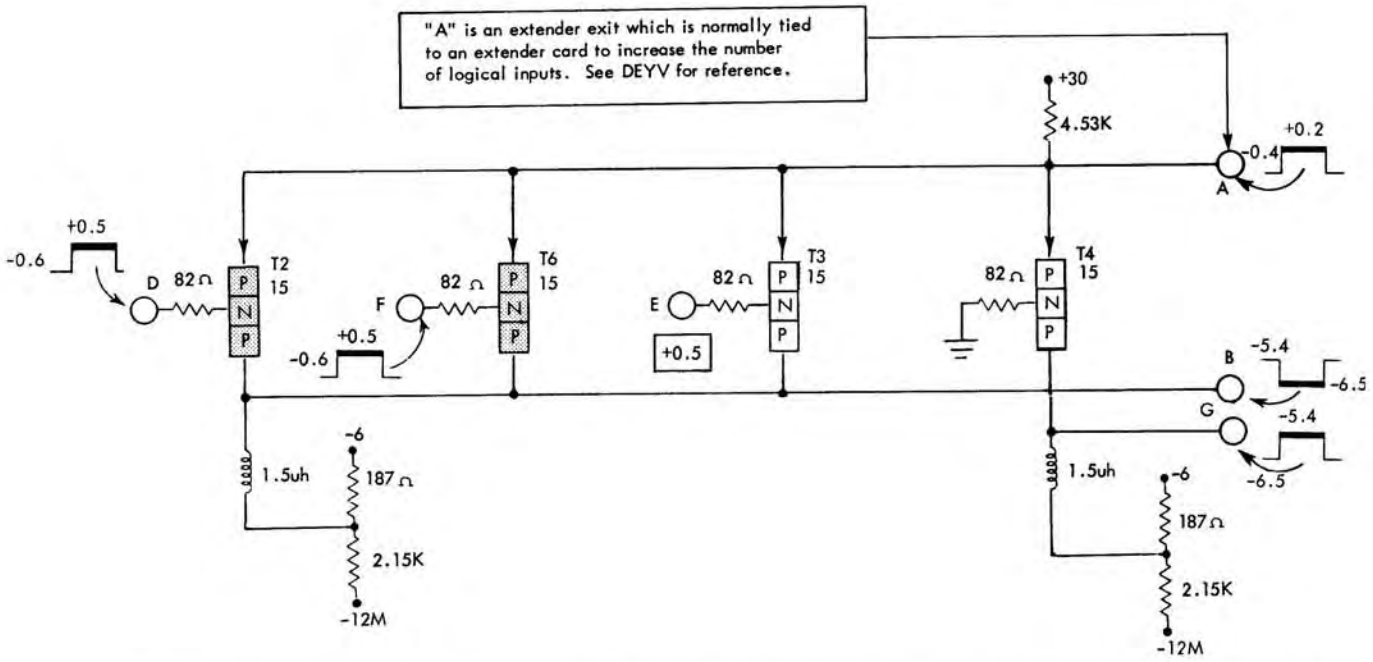

Card Code	Part No. 37----	Cplg Network In Ø	Cplg Network Out Ø	Circuit Used as		Input Levels Min.	Input Levels Max.	In Ø Output Min.	In Ø Output Max.	Out Ø Output Min.	Out Ø Output Max.	Ma. Output	In Ø	Out Ø	musec Block Delay Turn On	musec Block Delay Turn Off
DEZA	1321	Yes	Yes	+A	-O	+0.4	See driver for max. Output Levels	-5.6	-5.2	-5.6	-5.1					
DEYZ	1322	Yes	No	+AO	-OA							Min.	5.97	6.04	6	3
DEYY	1323	No	Yes	+TA	-TO	-0.4		-6.4	-6.5	-6.4	-6.5	Nom.	6.56	6.69	14	10
DEYX	1324	No	No									Max.	7.14	7.34	24	18

Diffused Junction Three-Way AND, Type B

The three-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of three +N inputs produces a +P in-phase output and a −P out-of-phase output. Output A is an extender exit.

Circuit Description

This circuit uses three transistors (T2, T6 and T3) in an AND configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (30v) supply. The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network, and output B is at a +P level of −5.4v because of current flow (6.7ma) out of its coupling network through T2 and T6 to +30v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output B falls to a −P level and output G rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v) so that transistor parameters are less critical.

Application

For some applications, the circuit driven by this logic block requires a coupling network other than the 187 ohm and 2.15K resistors shown. In such cases cap codes YX, YY and YZ are used as required (see chart). This circuit is also combined with an OR circuit to make up a trigger, and with other AND circuit blocks to obtain DOT functions.