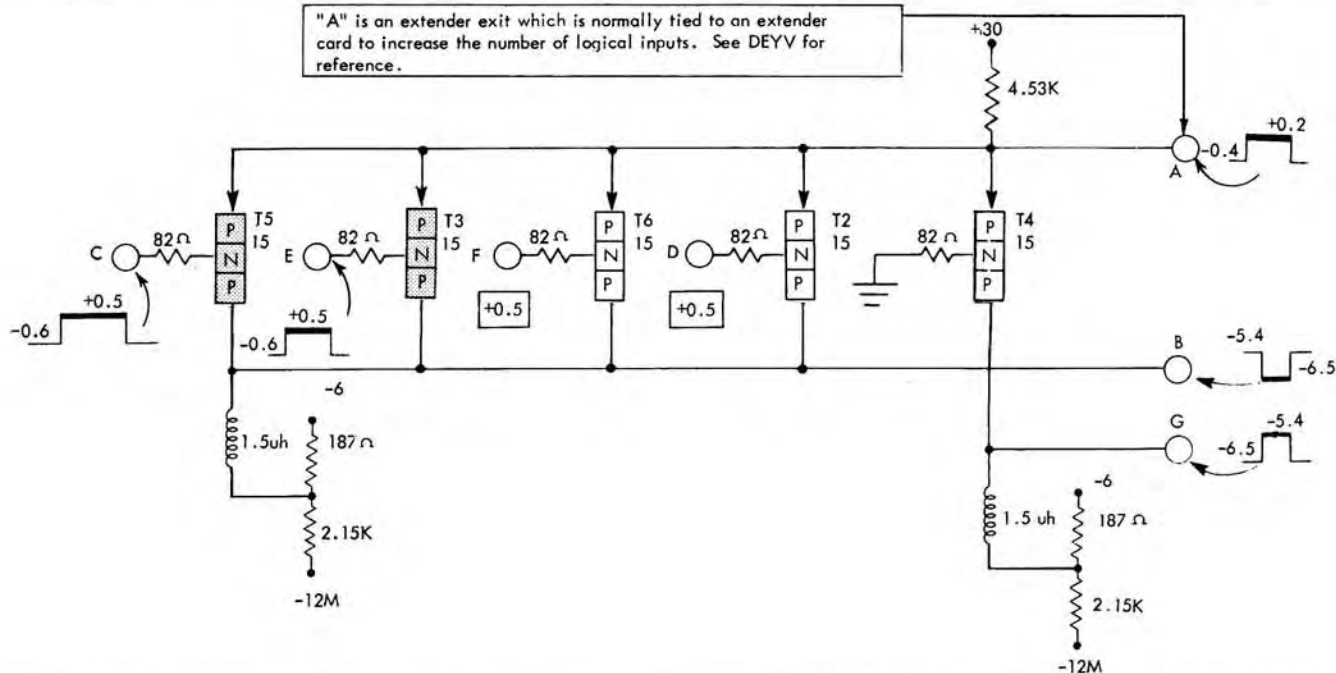


"A" is an extender exit which is normally tied to an extender card to increase the number of logical inputs. See DEYV for reference.



Card Code	Part No. 37----	Cplg Network		Circuit Used as		Input Levels		In $\emptyset$ Output		Out $\emptyset$ Output		Ma. Output		musec Block Delay		
		In $\emptyset$	Out $\emptyset$	+A	-O	Min.	Max.	Min.	Max.	Min.	Max.	In $\emptyset$	Out $\emptyset$	Turn On	Turn Off	
DEZJ	1314	Yes	Yes	+A	-O	+0.4	See driver for max Output Levels	-5.6	-5.2	-5.6	-5.1	Min.	5.97	6.04	8	4
DEZH	1315	Yes	No	+AO	-OA	-0.4		-6.4	-6.5	-6.4	-6.5	Nom.	6.56	6.69	15	9
DEZG	1316	No	Yes	+TA	-TO							Max.	7.14	7.34	24	15
DEZF	1317	No	No													

### Diffused Junction Four-Way AND, Type B

The four-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of four +N inputs produces a +P in-phase output and a -P out-of-phase output. Output A is an extender exit.

#### Circuit Description

This circuit uses four transistors (T5, T3, T6, and T2) in an AND configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (30v) supply. The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any -N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a -P level of -6.5v because of divider current through its coupling network, and output

B is at a +P because of current flow (6.7ma) out of its coupling network through T5 and T3 to +30v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output B falls to a -P level and output G rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v) so that transistor parameters are less critical.

#### Application

For some applications, the circuit driven by this logic block requires a special input coupling network. In such cases cap diodes ZF, ZG and ZH are used as required. This circuit is also combined with an OR circuit to make up a trigger, and with other AND blocks to obtain dot functions.