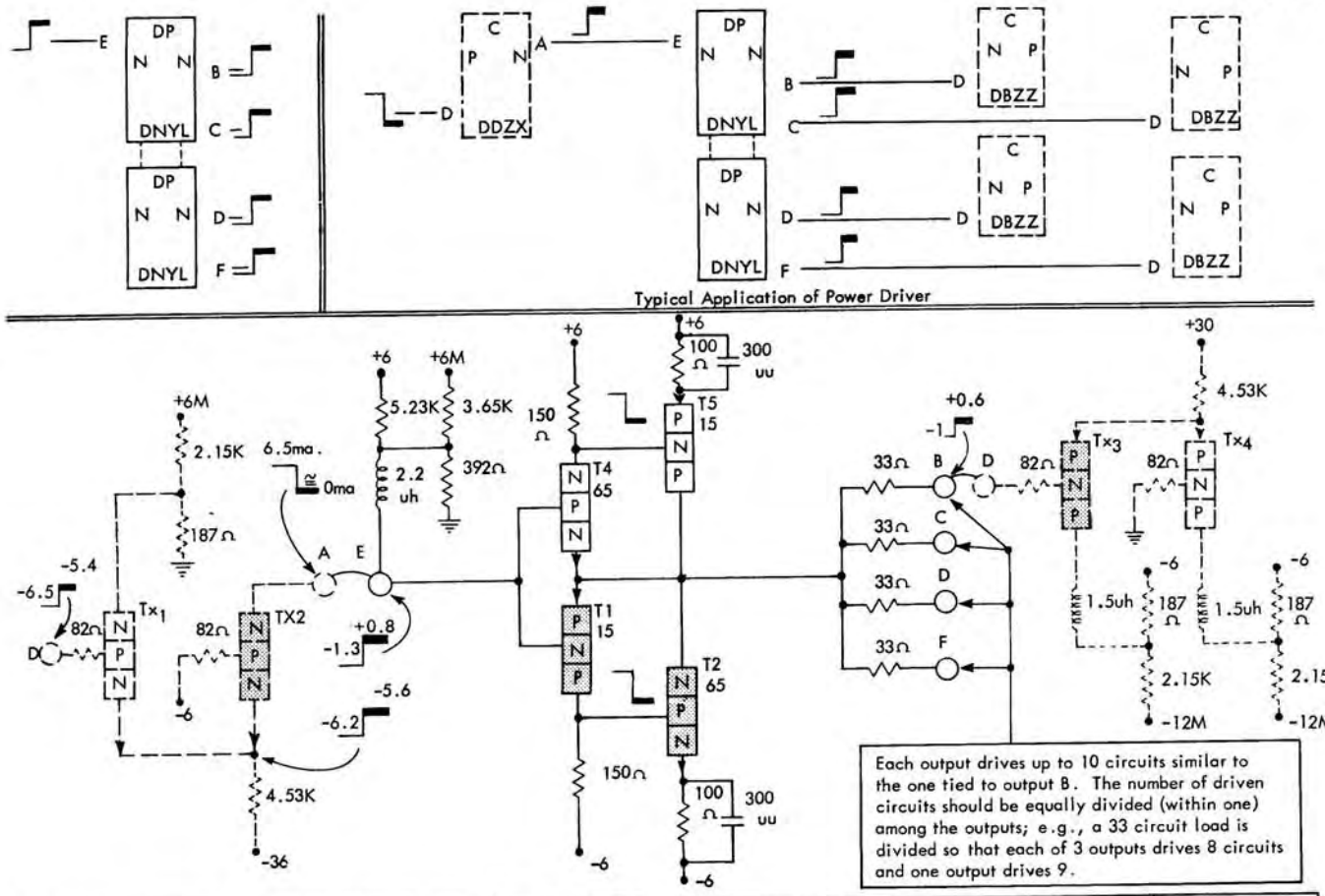

Card Code	Part No. 37----	Circuit used as	Input levels Min.	Input levels Max.	Output Levels Min.	Output Levels Max.
DNYL	1351	DP	-5.1 to -6.7	-4.3 to -6.9	-5.5 to -6.4	-4.3 to -6.7

usec Block Delay (Note 1)	Turn On	Turn Off
Min.	15	13
Nom.	31	21
Max.	45	31

Input Current Driven by	Min. Pulse Width
Type A Block, in Ø output	A ± drive pulse of 50 musec followed by a 100 musec recovery time.
Type A Block, out Ø output (only when DP input clamp is used)	
Type B Block, either output	

Note 1. Delays are measured from input terminal E of the power driver to the output of a logic block driven by the driver. The delays shown are those of the 4-10 base driver and are only approximate values for the 11-40 base driver.

Diffused Junction N-to-N Power Driver (11-40 Bases)

This power driver is used when it is required to drive from 11 to 40 bases (logic circuits of the type shown above.) It provides an in-phase N-line output for an N-line input. This driver is not designed to drive widely separated circuits. Because of the driving requirements of this circuit, a special network is built into its input. This network converts an input current into the N-line signal levels required. To keep skew of the output signal to a minimum, the length of output lines should be as equal as possible and the number of circuits driven by each line should be equal to within one circuit. (See note.)

Circuit Description

In the state shown, TX2 is forward-biased and 6.5ma flows from −36v through TX2 into the coupling network to +6v and ground. Current flow into this coupling network establishes the input level at −1.3v. T1 is forward-biased and its emitter clamps to the −1.3v input. Forward load current flows from −6v through T1, base-emitter diode of TX3's to +30v. Current through T1 develops a voltage drop across its 150 ohm collector resistor, which raises the base potential of T2 above −6v. Thus, T1 and T2 conduct in parallel and outputs B, C, D and F are at a −N level of −1v.

When the input to the converter rises, TX2 is cut off and the input current to the driver falls to zero. Divider current through the coupling network causes the input level to rise to +0.8v. When the input level rises above ground, T4 is forward-biased and T1 and T2 are cut off. The emitter of T4 follows its base above ground, which reverse-biases the TX3 load transistors. Back current from the load transistors flows out of the collector-base diode of the TX3's, through T4 to +6v. The collector potential of T4 falls, and forward-biases T5. Thus, T4 and T5 conduct in parallel and the driver output is at a +N level of 0.6v.

The input network peaking coil compensates for line capacitance so that optimum square-wave response is realized. The 33 ohm output resistance is an oscillation suppressor which is necessary because of the inductive coupling network used. The effect of output capacitance is reduced by using 300 $\mu\mu$fd bypass capacitors.