Current Mode, Negative Binary Trigger, Cards 1 and 2

The FF - - card and the FJ - - card are connected to form a negative binary trigger (see logic application). A +P to input E of FJ - - resets the trigger off; the in-phase output is +P and the out-of-phase output is −P. Each −N input to FF - - alters the trigger status, so the first −N input after reset turns the trigger on. The in-phase output falls to a −P and the out-of-phase output rises to a +P. Note that when the trigger is on, its in-phase output follows the sign of the function (−TB function has a negative sign and the in-phase output is negative).

The input signal in the logic application is a dashed square wave *current* input and an inductive AC voltage resulting from this current input (see note associated with input signal). Such an input is necessary because the design of a binary trigger requires that the trigger operate on AC signals only and be isolated from the DC component of the signals. The input inductive network is designed to develop a negative signal when the input current rises from zero. The fall of the current back to zero has no effect. The trigger is designed to operate at 1 megacycle.

Circuit Description

Before studying the circuit in detail, take an overall look at the schematic. Note the trigger status chart and sequence chart which summarize the over-all sequence of events. The trigger status chart shows that the trigger is on in the state shown (TF1, TF4, and TJ2 conducting).

The trigger is flipped by increasing input current from zero to 6ma. Input current flows from the negative source of the driving circuit into input H where it divides into two components of current. One component flows through 523 ohms and 3μfd in parallel and through 2.37K to +6v. The second component flows through the 27μh coil L3 to ground. It is the changing current through this coil which develops the 1.5v signal shown. This 1.5v signal is passed by the 3μfd capacitor and the forward bias of TF4 is reduced. The emitter of TF4 follows its base and TF3 conducts when its base falls below +0.2v. Current flows from −12v through TF3 and 681 ohms to +6v which raises the emitter of TJ2 above −6v and cuts off TJ2. With TJ2 cut off, current flow through coil L1 falls to zero and develops a 1v signal. The base of TF1 rises to a +1v which forward-biases TF2 and cuts off TF1. Current flows out of the coupling network and the delay line, through TF2 to +6v which establishes the in-phase output B at a +P level of −5.2v. Output E falls to a −P level of −6.8v because of divider current through the coupling network.

When the input signal to the base of TF4 times out and returns to +1.1v, current through TF4 is increased and the base of TF3 rises to +0.9v. Current flow through TF3 is reduced to zero and TJ4 is forward-biased when its emitter signal falls below −5.2v. Current flows from −12v through TJ4 and into L2 and D1 in parallel to ground which maintains TF2 forward-biased. D2 short circuits the negative excursion of the signal developed by L1. The time base of the signal developed by L1 is greater than that of the input network to insure that the base signal of TF2 is driven positive (current flows through TJ4) before the base of TF1 again falls negative.

The trigger is now off (in-phase output is +P) and remains in this state until a new current input signal is received. For a turn-on sequence, refer to the sequence chart. Reset is accomplished by a +P signal to input E which forward biases TJ3 and cuts off TJ2. With TJ2 cut off, TF1 cuts off and TF2 turns on.