Current Mode, Positive Binary Trigger, Cards 1 and 2

The FH - - card and the FG - - card are interconnected to form a plus binary trigger (see logic application). A −N level to input E of FG - - resets the trigger off; the in-phase output is −N and the out-of-phase output is +N. Each +P input to FH - - alters the trigger status, so the first +P input after reset turns the trigger on. The in-phase ouput rises to a +N and the out-of-phase output falls to a −N. Note that when the trigger is on, its in-phase output follows the sign of the function (+TB function has a plus sign and the in-phase output is plus).

The input signal in the logic application consists of a dashed square wave *current* input and an inductive AC voltage resulting from this current input (see note associated with input signal). Such an input is necessary because the design of a binary trigger requires that the trigger operate on AC signals only and be isolated from the DC component of the signals. The input inductive network is designed to develop a positive signal when the input current rises from zero. The fall of the current back to zero has no effect. This trigger is designed to operate at 1 megacycle.

Circuit Description

Before studying the circuit in detail, take an overall look at the schematic. Note the trigger status chart and sequence chart which summarize the over-all sequence of events. The trigger status chart shows that the trigger is on in the state shown (TG2, TH1, and TH4 conducting).

The trigger is flipped by causing current to input H to rise from zero to 6ma. This input causes one component of current to flow from −12v through 2.37K, 523 ohms and 3μfd in parallel to input H and to the positive return of the driving circuit. A second component of current flows from −6v through the 27μh coil L3 to input H. It is the changing current through this coil which develops the 1.5v signal shown. This 1.5v signal is passed by the 3μfd capacitor and the forward bias of TH4 is reduced. The emitter of TH4 follows its base and TH3 conducts when its base rises above −6.2v. Current flows from −12v through 681 ohms, and TH3 to +6v which lowers the emitter of TG2 below ground and cuts off TG2. With TG2 cut off, current flow through coil L1 falls to zero and develops a 1v signal. The base of TH1 falls to −7v which forward-biases TH2 and cuts off TH1. Current flows from −12v through TH2 into the delay line and coupling network which establishes the in-phase output B at a −N level of −0.8v. Output E rises to a +N level of +0.8v because of divider current through the coupling network.

When the input signal to the base of TH4 times out and returns to −7.1v, current through TH4 increases and the base of TH3 falls to −6.9v. Current flow through TH3 is reduced to zero, and TG4 is forward-biased when its emitter signal rises above −0.8v. Current flows from −6v through D1 and L2 in parallel and through TG4 to +6v which maintains TH2 forward-biased. D2 short circuits the positive excursion of the signal developed by L1. The time base of the signal developed by L1 is greater than that of the input network to insure that the base signal of TH2 is driven positive (current flows through TG4) before the base of TH1 again rises positive.
which forward-biases TG3 and cuts off TG2. With TG2 cut off, TH1 cuts off and TH2 turns on.

The trigger is now off (in-phase output is −N) and remains in this state until a new current input signal is received. For a turn-on sequence, refer to the sequence chart. Reset is accomplished by a −N signal to input E.