normally used in shift register operation. The read-out pulse is a constant current signal used to reset all cores to zero at A time of each cycle. A constant voltage read-in pulse occurs at C time to set a core if a read-in control driver is gated on. Data may be read into a shift register from other logic circuits by use of a bit insert driver or can be parallel transferred into the register.

Cycle 1 Serial Shift Right (Figure FX1). Assume that core position 2 is set on and it is necessary to move this information bit to the right to core position 3. At A time, the read-out driver (ROD) is gated on and provides a constant current pulse to the serially connected read-out windings and resets all cores off.

The read-out control driver (ROCD) for each position is gated on and sets the base level of all output transistors to +6.5v so that if a core is switched the transistors are turned on. When core 2 is flipped to the reset state at A time, about 5v is induced in the output winding of core 2, and T2 is forward-biased on. The 68 ohm collector resistor permits the transistor to saturate quickly, reducing the power dissipation within T2 and allowing the capacitor C2 to rapidly charge to +6 volts. The capacitor is shunted by a 27K resistor that insures that the capacitor is not charged by the I_{co} current through the transistor when it is held off. The capacitor is a temporary storage between read-out and read-in pulses and provides a means of sampling core status.

At read-in-time (C time), the right shift read-in driver (RIC) is gated on and provides a −6v output. Discharge current from −6v through the input winding of core position 3 to C2 (+6v) is sufficient to set core 3 on. Information from core 2 is serially shifted right from core 2 to core 3. During this same time core 1 and core 3 are read out and also shift information bits to the right if they originally contained a stored bit.

Cycle 2 Serial Shift Left (Figure FX-1). Assume that core 2 is set on and it is necessary to shift the information to the left to core 1. Circuit operation for the read-out of core 2 and the charging of C2 are identical to those of cycle 1. At A time all circuits are reset off. With the ROCD on (+6.5v), T2 conducts and charges the capacitor (C2) to +6v. At read-in time, however, the serial left shift read-in control is gated on and provides a −6v output. Conduction through the left shift input windings of core 1 to C2 discharges the capacitor and sets core 1 on. Thus, information from core 2 was shifted left to core 1.

Cycle 3 Regeneration (Figure FX-1). In normal operation, a constant read-out and regeneration feature allows dynamic sensing for indicators and sampling. Again, assume core 2 is set on. At read-out time all cores are reset off. With the ROCD on, the voltage developed in the output winding is enough to drive T2 into saturation and charge C2 to +6v. At read-in time, the regeneration read-in driver is gated on and provides a −6v output. Discharge current through the regeneration input winding of core 2 discharges C2 and sets core 2 on. Information was read out for sampling and then read back into its original core position.

Serial-Parallel Transfer (Figure FX-2). Serial transfer takes place within a given register. Parallel transfer moves the entire contents of one register to the bus capacitor storage circuits, where the information can be sampled or transferred to another register. To parallel transfer between registers it is essential that the registers share common bus capacitor storage circuits.

The theoretical circuit shown in Figure FX-1 cannot accomplish both serial and parallel transfer of information. By adding a second output circuit and an additional input winding to each core position, both types of transfers are accomplished.

Figure FX-2 shows a portion of two shift registers that share common bus capacitor storage circuits. The core positions shown are bit positions within a particular digit of information (for example, 0 bit positions of digits 1 and 2).

A parallel transfer of information bits between register I and register II is made as follows. Assume core 1 of shift register I is set on and it is desired to parallel-shift this information bit to core 1 of shift register II. At read-out time all core positions are reset off. Register I serial ROCD and bus ROCD circuits are on (+6.5v) and permit both transistors (T1 and T2) to conduct when core 1 is reset off. Current flow to the serial capacitor C1 and to the bus capacitor C2 charges both capacitors to +6v.

Because register II is to receive the information from register I, it must be cleared during the read-out cycle. This requires that both the serial ROCD and bus ROCD for register II remain off (+12v).

Thus, at read-out time the cores of register II are reset without charging any capacitors because the transistors are held reverse-biased off.

At read-in time, the bus read-in control for register II is turned on (−6v), allowing current flow through the bus input winding of register II (core 1), the isolation diode, to C2 to discharge the capacitor and set core I of register II. Also during read-in time, the information bit stored in C1 of register I may be either regenerated back into core 1 or serially shifted as described previously. On the parallel transfer, if a read-in driver is not gated on to discharge the bus storage capacitor, a special parallel clear line is gated on each cycle to discharge the capacitors. This action prevents the transistor I_{co} from charging the capacitor after a given period of time.

Application

The magnetic core shift register system described is designed to handle the ten-digit 2-of-5 bit word transfers in the 7070. Other coding arrangements and register sizes are possible as long as the driver ratings are not exceeded.