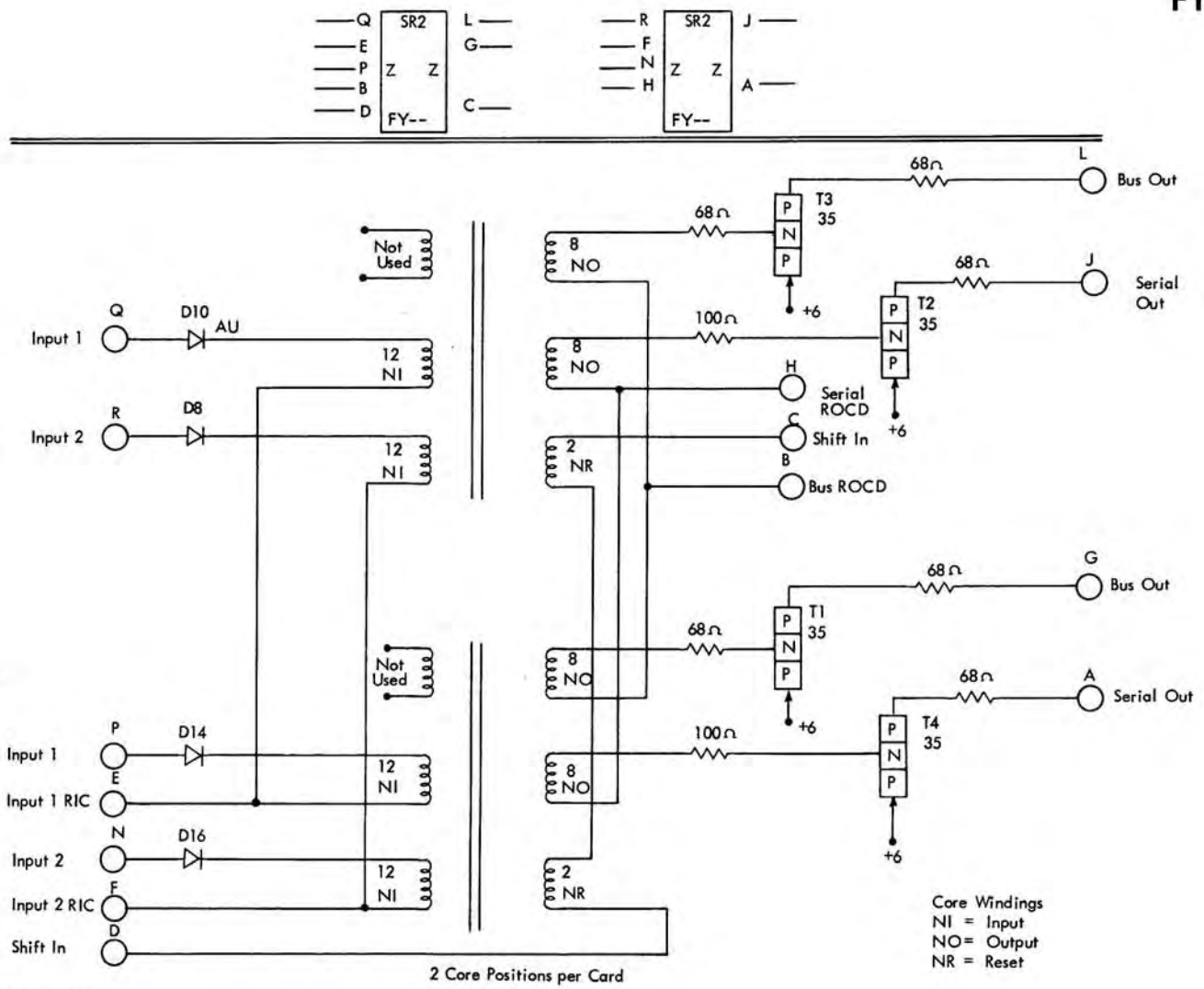


FY-- 371507

The FY-- is used to expand the inputs to the FX-- card.

### Magnetic Core Shift Register Extender SR2

The FY - - card expands the number of inputs to the FX - - card. Two magnetic core positions are mounted on each card; each position is capable of storing one bit of information. Each core position contains two input windings, two output windings, and a reset winding.

The input windings are driven by core mode Z lines from either a capacitor storage network or from a special bit insert driver. These input windings are gated on by selecting the read-in driver circuits (HG - - or GZ - - card).

Normally, all the reset windings of a shift register are serially connected and receive a constant current read-out pulse from a read-out driver (GY - - card). The output windings are biased by a read-out control driver (HF - - card), which controls the bias level of the output transistors.

*Circuit Description* (Extender Operation)

Figure FY-1 shows a part of the SR2 card extending the inputs to an SR1 card. Note that the serial and the bus outputs of the two cards are commoned and feed the register capacitors of the SR1 card. The two core positions function as a single core with an increased number of inputs.

During cycle 1 (Figure FY-1) the read-out driver (ROD) is gated on and resets both core positions to the off status. At this time, the serial and bus read-out control drivers are off for both the SR2 and SR1 output windings and prevent the output transistors from turning on. C1 and C2 remain discharged.

At read-in time, the bit insert driver and the read-in control (RIC) of the SR2 core input winding are gated on. Enough current flows through this winding to set the SR2 core on. All read-in controls for the SR1 core remain off during this cycle.

The ROD is again turned on in cycle 2 and resets both cores off. The serial and bus read-out control for the SR2 core are now on. When the SR2 core is switched off, about 5v is induced in the output windings. T1 and T2 are biased on and charge the bus and serial capacitors associated with the SR1 card to +6v. At read-in time of cycle 2, the capacitors are discharged to regenerate the information bit in the SR1 core, or the information bit may be serial or parallel transferred to another core position.

A bit was thus read into the extender core during cycle 1 and transferred to the register card during cycle 2.