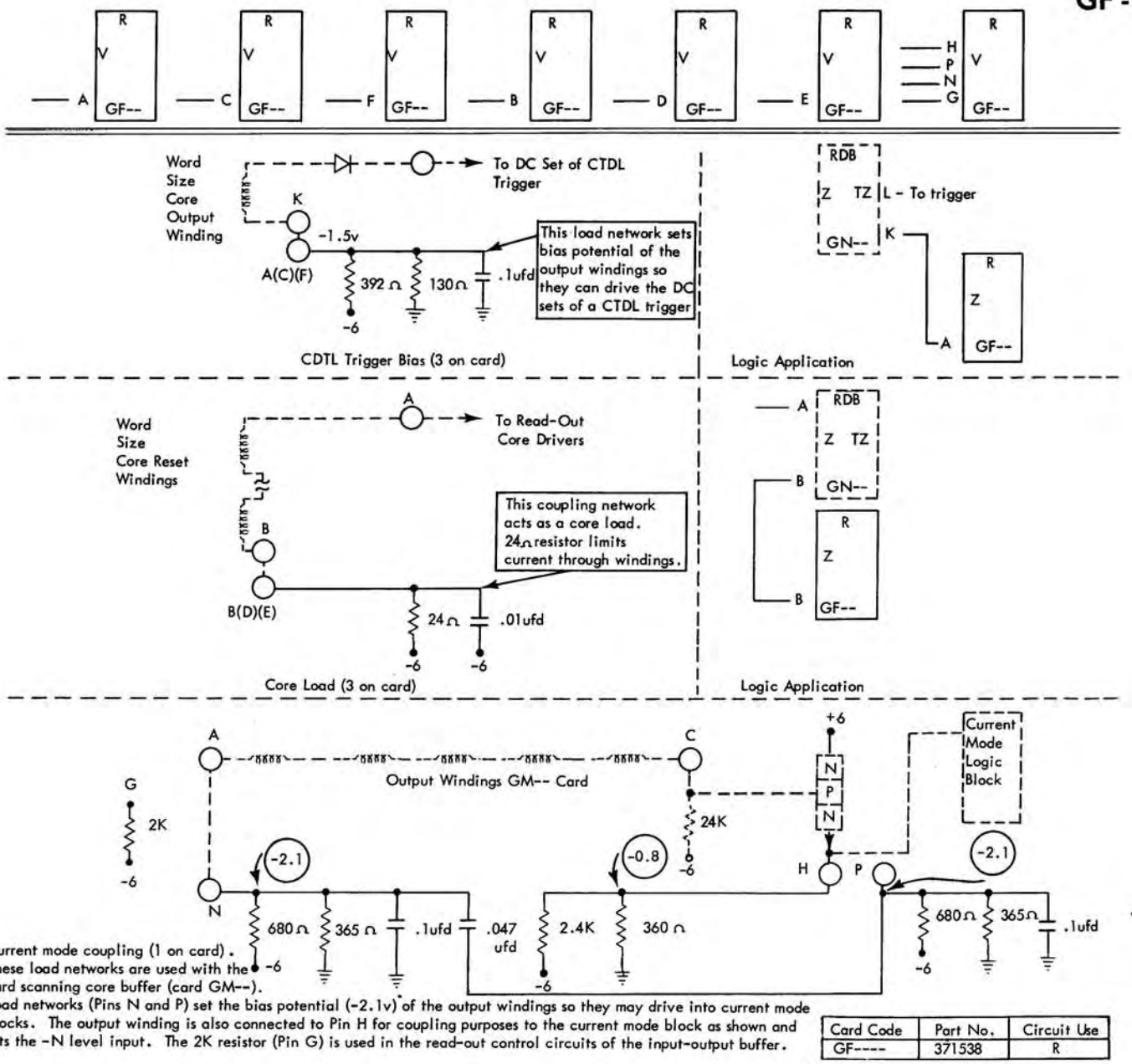

Current mode coupling (1 on card). These load networks are used with the card scanning core buffer (card GM--).
Load networks (Pins N and P) set the bias potential (-2.1v) of the output windings so they may drive into current mode blocks. The output winding is also connected to Pin H for coupling purposes to the current mode block as shown and sets the -N level input. The 2K resistor (Pin G) is used in the read-out control circuits of the input-output buffer.

Card Code	Part No.	Circuit Use
GF----	371538	R

Bias, Load, and Coupling Networks

The GF - - card consists of seven resistor-capacitor networks designed for use with the magnetic core input-output buffer cards. These networks serve as bias, load, and coupling circuits for the various windings and circuitry associated with the output core cards.

Circuit Description

Typical applications of these networks are illustrated. Circuits with input pins A, C, and F are usually tied to the output windings of the word-size core card (GN - -). The output windings are biased at −1.5v by the divider network. When the core is switched, about 5v is induced in the output which is enough to overcome this bias and to permit direct drive to CTDL trigger circuits. The 0.1μfd capacitor filters transient spikes caused by core switching.

Circuits with input pins at B, D, and E serve as core loads that limit the current through the core windings. The 0.01μfd capacitor across the 24 ohm resistor, filters the transient spikes resulting from core switching.

In the card scanning core buffer application (GM - - card), additional networks are used to obtain a current mode output for driving into logic circuits. The output windings are biased to −2.1v by the connection to pin N or pin P. When a core is switched, about 5v is induced in the output windings. This voltage is enough to overcome the bias potential of the output windings and gives a current mode signal at the base of the transistor. The transistor is normally biased off, because the emitter load (pin H) is set at −0.8v. When the core is switched, the transistor turns on and the current mode output drives into the logic blocks. The 0.047 μfd capacitor between the divider networks stabilizes the voltage at pin N and pin P. The 2K resistor (pin G) is used as a load for the read-out core drivers (not shown above, see GLVH or GLVG cards).