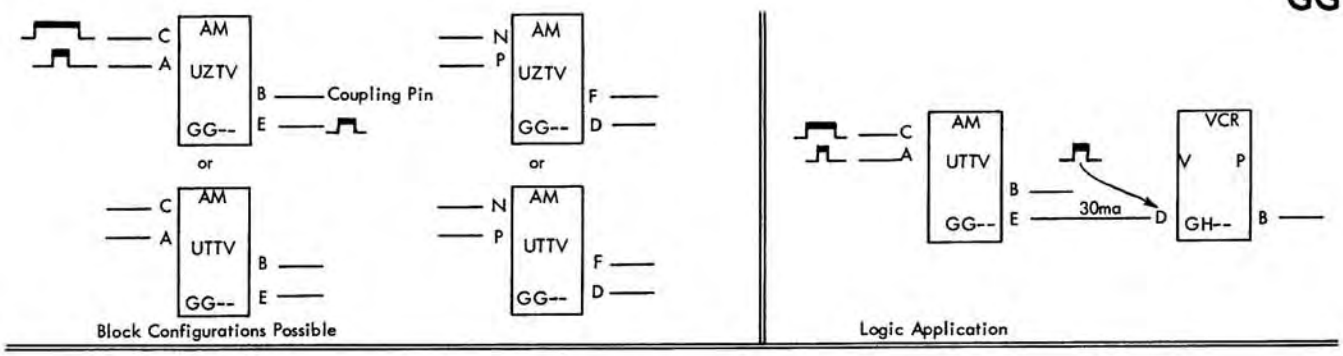

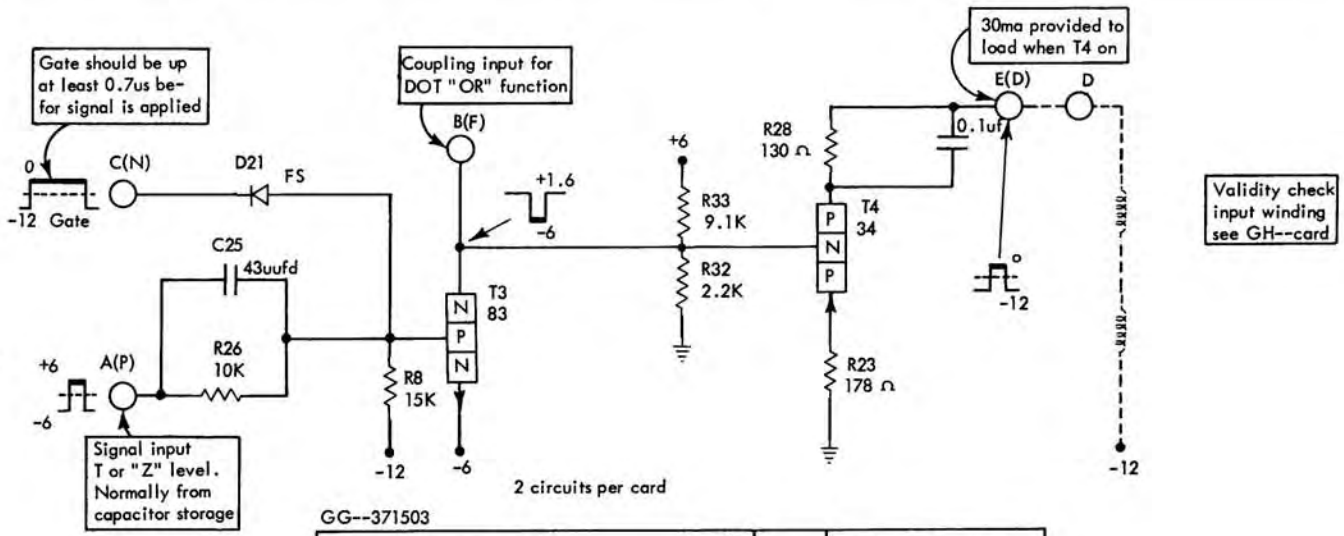

GG--371503

Input Levels						On Output Current	Delays (usec)		
Gate "U" Line		Signal "T" Line		Signal "Z" Line				Per	Circuit
Min.	Max.	Min.	Max.	Min.	Max.				
-5.5	+0.2 to -7.4 / -12.5	2.7	6.2 to -4.0 / -6.2	2.7	6.2 to -4.0 / -6.2	30ma	Turn On	Min.	0.1
								Max.	0.35
							Turn Off	Min.	0.2
								Max.	1.1

Capacitor Sense Amplifier and Driver

The capacitor sense amplifier and driver is used to sense the core register level or amplify a CTDL T line.

There are two identical sense circuits on the GG - - card. Both the gate input and signal input must be up to obtain 30ma of drive current in the output circuit. These drivers supply the current to validity check circuits or to modified core register positions.

The U level gate input (pin C) is driven by a CTDL logic block or an emitter follower and controls the bias potential at the base of T3. The gate is set 0.7μs before the signal input is applied at pin A. Values for the gate and signal inputs are shown on the circuit diagram.

Circuit Description

Gate Down-Signal Input Up or Down. Assume that the signal input is up (or down) and the gate input is down (−12v). Conduction through D21 and R26 sets the base of T3 to the −12v gate level. T3 is reverse-biased and off. With T3 off, the collector goes to 1.2v which is set by the divider network of R32 and R33. T4 is reverse-biased off and no current flows in the output circuit.

Gate Up-Signal Input Up. When coincidence of the up gate level and the up signal level occurs, conduction through R26 and D21 drops the base level to 0v. T3 becomes forward-biased and conducts. The collector of T3 drops to −6v and forward-biases T4 on. With T4 on, 30ma of current is supplied the output load. The divider network of R33 and R32 acts as a speed-up network and prevents T4 from being reverse-biased too far in the off direction. This divider also limits the amount of reverse voltage across the collector to the base junction of T4 during the reset time of the validity check circuit.

Application

These drivers furnish 30ma of current to a modified core register circuit or to a validity check circuit when the input winding of these circuits is returned to −12v.

A DOT OR function is performed by coupling unloaded capacitor sense amplifier outputs to pin B. A maximum of two capacitor sense amplifier circuits may be coupled to provide a three-way OR function driving into T4 (see HBWW cards).