Magnetic Core 2-of-5 Bit Validity Check Cards

The GH - - cards are found in validity check circuits. These circuits check for valid information, coded in the 2-of-5 bit code, on either a serial or parallel transfer of information. Three circuits are located on each card, two sensing circuits and one coupling circuit. The two sense circuits are identical, each consisting of two magnetic ribbon cores and a diode "mix." The coupling circuit is composed of a resistor network and a diode switch.

The validity check circuits (VCK) furnish a 2μs −P output for a valid input of two and only two bits, and a +P output for an error condition due to an invalid input of more or less than two bits. For each digit position to be checked, five capacitor sense amplifier drivers (CG - - card) are coupled together to feed the input windings of the VCK card. Each amplifier that senses an information bit provides 30ma to the VCK input. The total to the VCK input sets either an error or no-error condition of the output P line.

Core Bias and Setting. In the static state, about 50ma of current flows through the bias windings of core 1 and core 2. This current biases core 1 such that 60ma or more must flow through its input winding to switch core 1. Core 2 is biased such that 90ma or more is required to flow through its input winding to switch its state. When the cores are switched, 2v is developed across their output windings. The DOT end of the output winding is negative at this time. Since each amplifier supplies 30ma of current when impulsed by an information bit, the status of core 1 and core 2 in relation to the number of bits sensed is given in the chart above. Notice that a −P output is available only when two bits are sensed, a valid input.

Circuit Description

To simplify circuit description, only circuits 1 and 3 of the VCK are shown above. The operation shown is for valid information only.

MISSING BITS

No Bits Sensed. Assume that none of the sense amplifiers are impulsed and that no current flows through the input windings. The voltage divider R11 and R9 connected between −6v and ground sets a −5v reference level at pin A. Voltage divider R13 and R15 connected between −6v and −12v sets pin H at a −7v reference level. D32 and D33 perform an OR function and D8 and D17 perform an AND function.

With no current flowing through the input windings, neither core 1 nor core 2 is switched, and no voltage is developed across the output winding. The voltage at point Y is −5v and at point Z, −7v. The output (pin B) from the OR circuit is −5v. This voltage also appears at pin N through the AND circuit, as both legs of the switch are at −5v. Thus, with no information sensed, the output is a +P line indicating an error condition.

One Bit Sensed. The circuit operation is the same if only one bit is sensed. The sense amplifiers provide only 30ma of current through the input windings, which is insufficient to switch the cores. A +P line output is again obtained.

CORRECT OPERATIONS

Two Bits Sensed. When two information bits are sensed at the sense amplifiers, 60ma of current flows through the input windings and is sufficient to switch core 1 only. The two volts developed across the output windings of core 1 is of such polarity as to drop point Y to −7v. Point Z remains at −7v because core 2 was not switched. The OR circuit output is now −7v and appears at pin N through the AND circuit. This −P output level indicates a no-error condition.

EXTRA BITS

Three, Four, or Five Bits Sensed. When three or more bits are sensed at the sense amplifiers, current flow (90ma to 150ma) through the input windings is sufficient to switch both core 1 and core 2. The polarity of the two volts developed across each output winding sets point Y at −7v and point Z at −5v. The duration of the voltage developed across the output winding of core 2 is longer than that developed across the output winding of core 1. The overlap is required to insure that the voltage at point Z (−5v) inhibits the −7v at point Y which would give a no-error indication. The −5v output from the OR circuit again gives a +P output level at pin N to indicate an error condition. D22 clamps point Y at −7v when core 1 is switched and D20 clamps point Z at −5v when core 2 is switched. L5 is used to damp out transient spikes caused when the cores are switched.

The turn-on delay, measured from the time the input of the sense amplifier crosses the 0v reference level until the VCK output crosses the −6v reference, is about 0.25μs.

Application

VCK cards are used for validity checking on all 2-of-5 bit coded channels such as adder entry, adder output, register, and tape synchronizers. In a parallel validity check application (Figure GH-1), up to 11 validity check circuits are coupled to give a single error indication. The outputs from each validity check sense circuit (pins B and C) are all connected to pin G of one card. Pins A and H of each VCK card used must be coupled to insure that there is no voltage shift in the reference voltages. The error no-error output for all digits checked is at pin N.