Inverter Core Driver

This card consists of three inverter core driver circuits, each capable of supplying 280ma to set magnetic cores. Turn-on of the core driver circuits depends on the voltage to which the transistor emitters are returned. The recommended procedure for coupling is with the emitter tied to ground and the collector load returned to −6v. This arrangement allows a CTDL T line from a loaded collector stage to control the driver.

Circuit Description

In a static condition, Ico flows through the pull-up resistor R26 and sets the base level of T4 to at least +0.54v. If a +T input (+6v) is applied to pin E, T4 remains reverse-biased off and the collector voltage is at −6v. No current flows in the load. When a −T input (−6v) of at least 1 microsecond duration is applied to pin E, T4 is forward-biased on and drops the output voltage to ground potential. Up to 280ma now flows through the core winding and is enough to set the magnetic core. R25 determines the base current supplied by the previous stage and C30 acts as a pulse shaper and improves the rise time of the output signal.

Emitter Follower Core Driver

The GLVH card consists of three emitter follower core driver circuits. Each circuit provides up to 315ma to set magnetic cores. The recommended procedure for coupling is with the collector tied to −6v and an emitter load of 1.3K to 3K returned to ground.

Circuit Description

In the static condition, Ico and Ibeo flows through R26 and sets the base level of T4 to at least 0.54v. With a +T input at pin E, minimum current flows through the emitter follower and the load. When a −T input (−6v) of at least 1 microsecond duration is applied to pin E, up to 315ma flows through the load to set the magnetic core.

Relay Driver

The GLVG card consists of three relay driver circuits that translate a T line input to a W line output. Each circuit is driven from an unloaded CTDL block and provides up to 280ma to a 20v relay or functional coil. This circuit also drives into tape wound cores. Recommended operation is with the emitter connected to ground and the collector load returned to −20v.

Circuit Description (Relay Load)

In the quiescent status, Ico current flow through the pull-up resistors R26, R25, and R21 to +6v keeps T3 reverse-biased off. The collector is at −20v and no current flows to the relay. When the input decreases to −6v, T4 is forward-biased on and the output at pin D increases to ground potential. Up to 280ma flows in the output circuit and picks the relay. A +T input turns off the transistor and current flow to the relay ceases. D1 clamps the collector voltage to −20v and prevents the inductive kick-back voltage from damaging the transistor. R21 serves as the collector load for the previous stage. C30 improves the waveshape of the output current pulse.

Pulse Duration

Input pulse duration is a function of the pick time of the relay used. The relay driver is normally fed by a CTDL latch circuit that provides an input pulse of at least 4 milliseconds for picking the relay. Drop out occurs when the latch is reset.