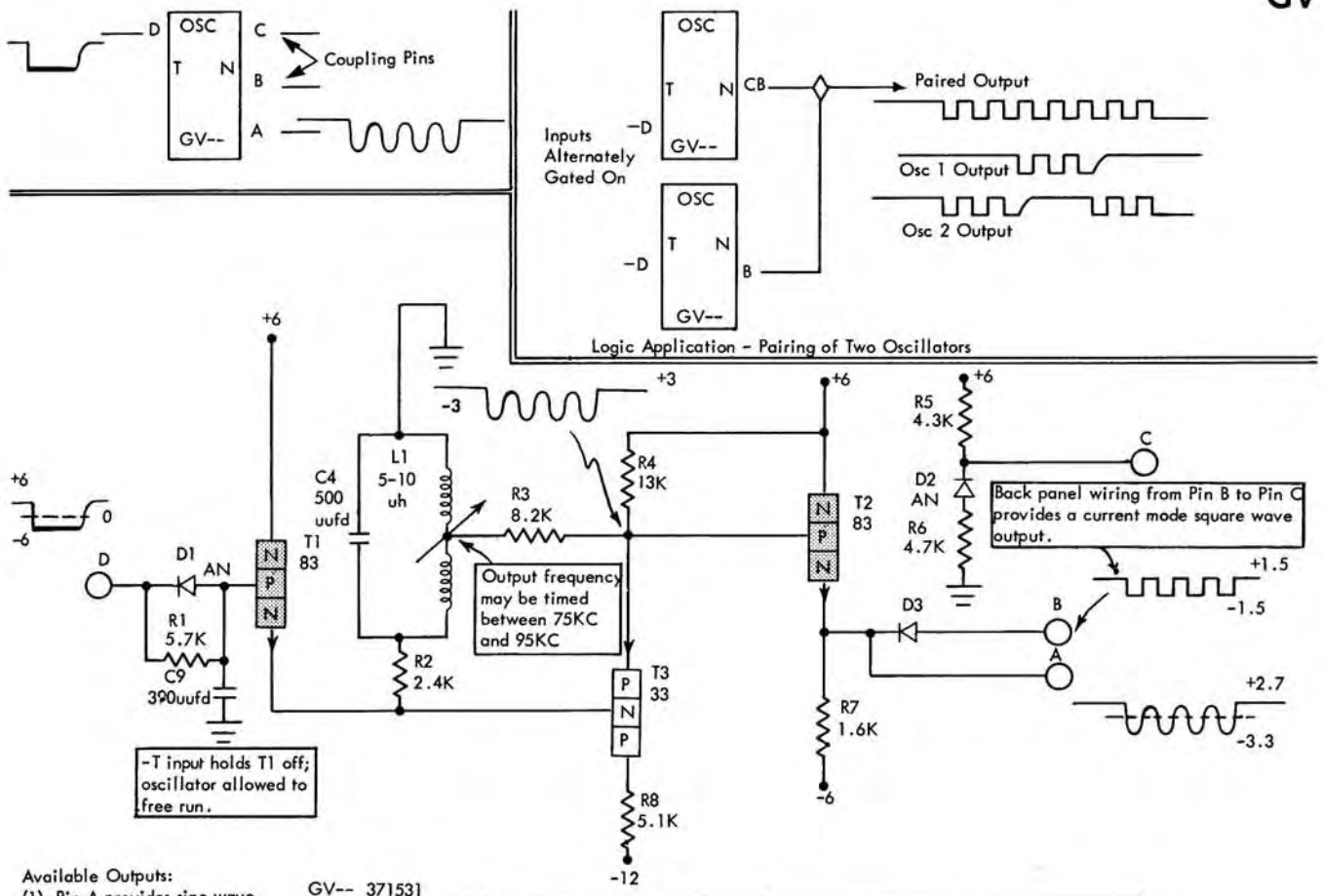

Available Outputs:
(1) Pin A provides sine wave CTDL output.
(2) Connection of Pin B to Pin C provides a current mode square wave output.
(3) Oscillators may be paired as shown in logic application. More stable operation results in output.

GV-- 371531

Input Levels		Output Levels				Delays		(Usec)
		Current Mode		CTDL			Per	Circuit
Min.	Max.	Min.	Max.	Min.	Max.			
5.8 / -5.8	6.2 / -6.2	1.63 / -1.0	1.9 / -2.0	2.3 / -3.0		Turn On	Min.	.10
							Max.	.20
						Turn Off	Min.	1.9*
							Max.	

* See Circuit Description

Variable Gated Oscillator

The GV - - card contains a variable gated oscillator which provides repetitive output pulses at a frequency of 75kc to 95kc. The circuit consists of a controlled input circuit, a Hartley type oscillator, and a buffer circuit. A special clamping network is provided on the card to permit paired coupling of two oscillator card outputs or to obtain either a CTDL T line or CM N line output. A down T level at pin D allows the oscillator to be free running and gives a sine wave output at pin A. This circuit is used as a read-write control for RAMAC® and operates at 83-1/3kc for this function.

Circuit Description

Input Up. Assume that the input T line is up at pin D. T1 is forward-biased and current flows through L1, R2 and T1. This sets the base level of T3 to +5.7v. The emitter of T3 is set near 3.0v by the divider network of L1, R3 and R4 to +6v. T3 is reverse-biased and the oscillator is off. Pin A output now is about 2.7v.

Input Down. When the input drops to −6v, T1 is reverse-biased and off. The negative swing to −6v causes T3 to be forward-biased on. Electron flow through R8, T3, R3, and the upper part of L1 to ground starts the oscillator action of the tank circuit. Magnetic feedback between the two sections of L1 is sufficient to keep the tank circuit oscillating, which provides regenerative feedback to the base of T3. The sine wave output from the tank circuit is coupled to emitter follower T2 and provides a sine wave output at pin A. Oscillations continue until T3 is cut off by a +T level input at pin D.

The frequency of oscillation is determined by the value of C4 and L1. The input diode D1 provides a quick turn-off of T1 while C9 is used to increase the turn-on time of T1. This increase in turn-on time (1.9μs) is desirable in order to insure overlap between the outputs of a pair of oscillators being alternated and mixed. D3, D2, R5 and R6 provide a special divider network that limits the CTDL output to a current mode N line.

The turn-on delay is measured from the time the input signal crosses the 0v reference until the first negative swing of the output crosses the 0v reference level.