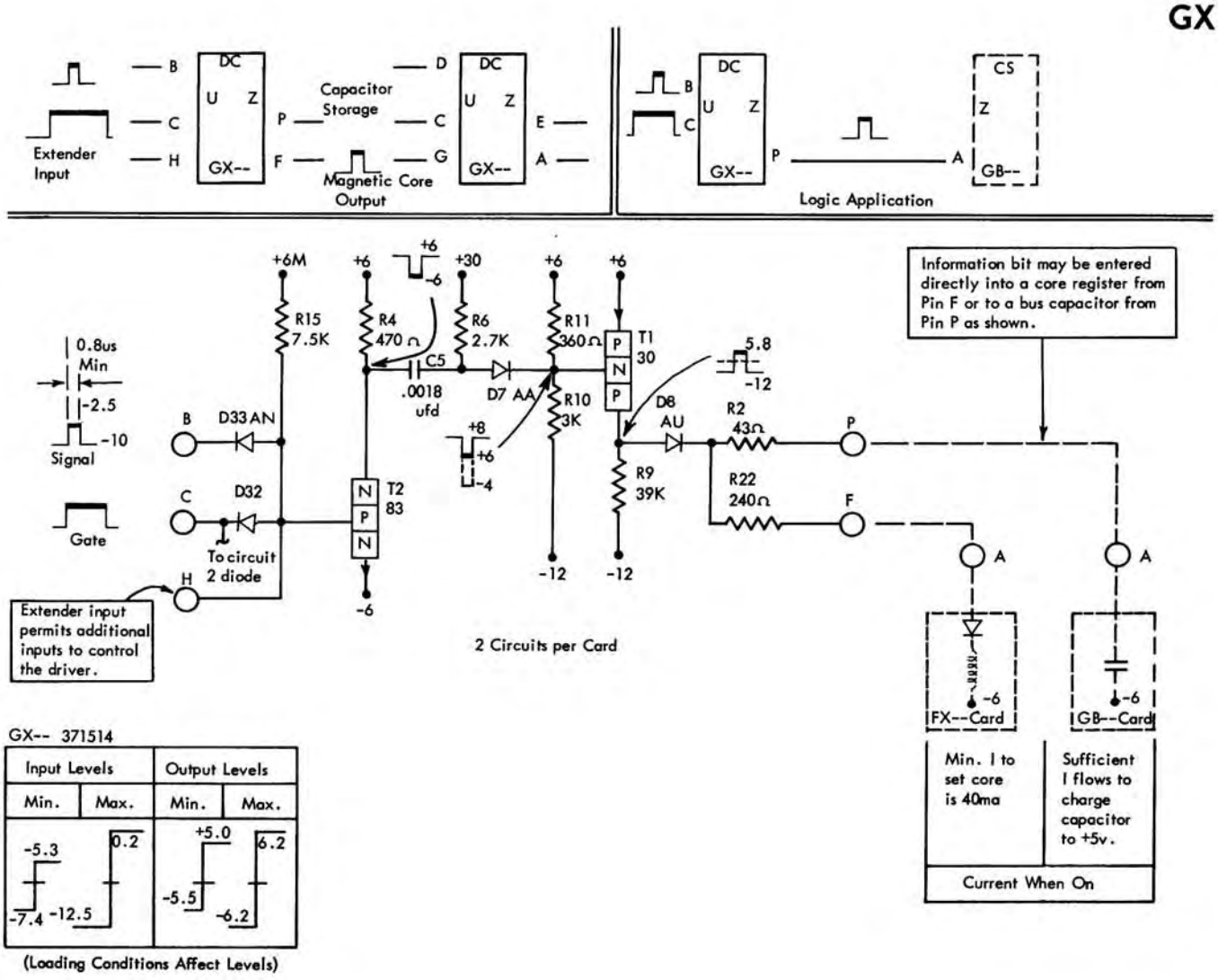

GX-- 371514

Input Levels		Output Levels	
Min.	Max.	Min.	Max.
-5.3 to -7.4	0.2 to -12.5	+5.0 to -5.5	6.2 to -6.2

(Loading Conditions Affect Levels)

Magnetic Core Bit Insert Driver

The GX - - card consists of two capacitor or core bit insert drivers. Each circuit provides the necessary current to set a magnetic core shift register directly or charge a bus capacitor storage circuit to the one state. Input arrangement to the circuit is similar to a CTDL logic block, consisting of two diode inputs and an extender pin. A +U signal of at least 0.8μs duration is required at both pins B and C to have the circuit turn on and provide a +Z output pulse of 1.45μs duration at pins P and F. Pin P is used when driving into a capacitor storage load; pin F is used when driving into a magnetic core input winding.

Circuit Description

A −U input at pin C (gate) or at pin B (signal) reverse-biases T2 off, and causes the collector voltage of T2 to be at +6v. Divider action of R11, R10, D7 and R6 sets the base of T1 to approximately +8v. T1 is biased off and its collector voltage is near −12v. No output current flows because the isolation diode D8 is reverse-biased.

Coincidence of +U inputs at pins B and C drives T2 into saturation and drops its collector voltage to −6v. The negative pulse (−12v) is coupled through C5 and turns T1 on. The current flow from the load through the forward-biased D8 and T1 to +6v is sufficient to charge a maximum capacitor storage load of 3500$\mu\mu$fd to +5v. If the output at pin F is used, a minimum current flow of approximately 40ma is required through the input winding to set a magnetic core position.

The coupling capacitor C5 also serves as a protective measure for T1 and the register core windings. If the input is "locked on," the negative shift coupled to the base of T1 lasts only for the RC time duration of the input network to T1. After a given period of time, T1 would return to its reverse-biased state and the power dissipation limits would not be exceeded in T1 or the core windings.

Application

In the 7070 system, the bit insert driver is used to enter information bits to a register core at C pulse time or to a bus capacitor at A pulse time.