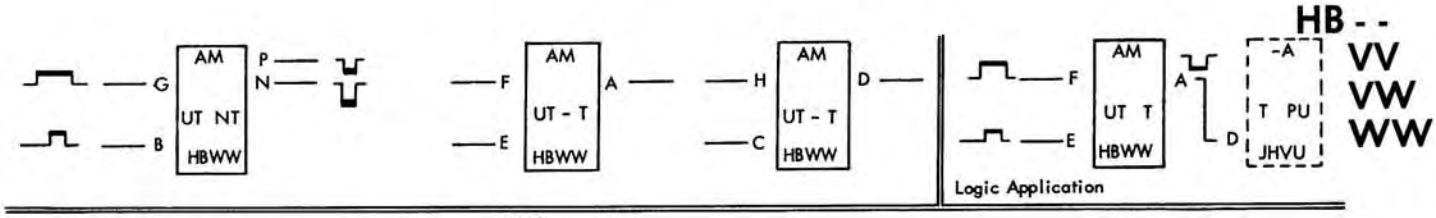

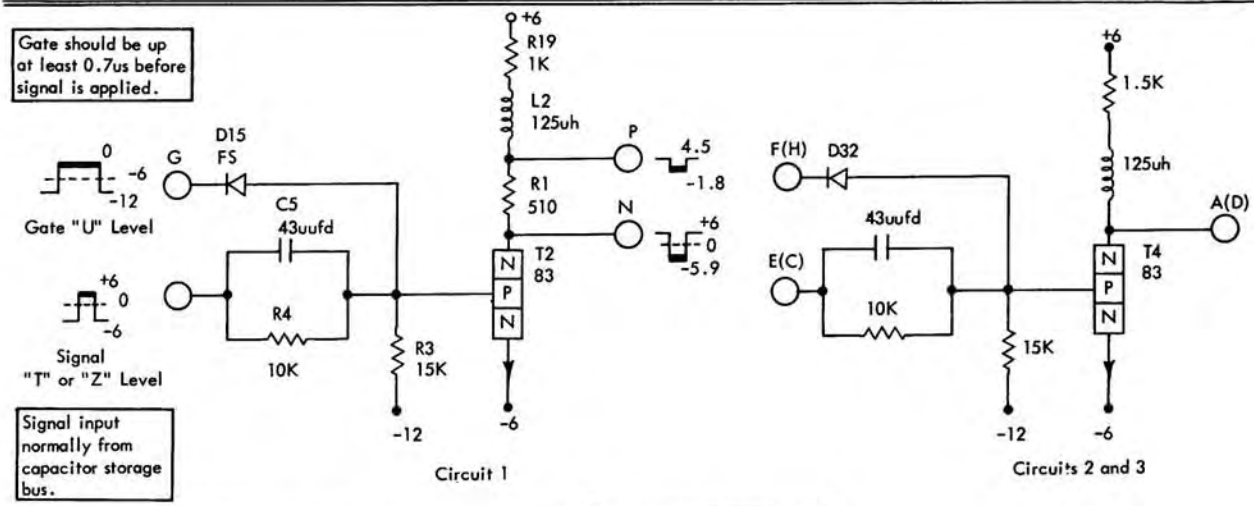

Input Levels			
Gate In		Signal In	
Min.	Max.	Min.	Max.
2.7 to -4.0	6.2 to -6.2	-5.5 to -7.4	0.2 to -12.5

Output Levels			
Current Mode		CTDL Out	
Min.	Max.	Min.	Max.
2.8 to -1.1	6.2 to -2.5	1.4 to -5.6	+6.2 to -6.2

Card Code	Part No 37----	CM Output Circuit	Collector Loading Circuit 1	2	3	Delays		(usec)
							Per	Block
HBWW	1500	1	Yes	Yes	Yes	Turn On	Min.	0.0
HBVW	1559	1	Yes	Yes	No		Max.	0.07
HBVV	1560	1	Yes	No	No	Turn Off	Min.	0.2
HB--	1561	No	No	No	No		Max.	0.55

Capacitor Sense Amplifier

The capacitor sense amplifier circuits are used to sense the capacitor levels of magnetic core registers or to invert a CTDL T line. Three capacitor sense amplifier circuits are located on each HBWW card. Both the gate input and signal input must be up for the transistor turn-on. The U line gate input is driven by CTDL logic blocks or emitter followers and must be up approximately 0.7μs before the signal input. The gate input controls the base bias level. An out-of-phase T level is obtained from these circuits.

Circuit Operation (Circuit 1)

Gate Down, Signal Up or Down. With a −U level at the gate input pin G, the base of T2 is held reverse-biased off regardless of the status of the input signal at pin B. The CTDL output at pin N is at +6v (no load).

Gate Up, Signal Up. When the gate input at pin G increases to 0v, and the signal input at pin B is up (+6v), conduction through D15 and R4, and R3 and R4 forward-biases T2 on. The output voltage at pin N is approximately −6v (minus the small drop across the forward-biased transistor). C5 couples the input signal to the base of T2 and improves the output waveform. The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current mode output.

Application

These circuits are normally used to sample the status of the capacitor levels of magnetic core registers.

The circuit loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. DOT functions are accomplished by connecting similar output pins together to share a common collector load. CTDL and current mode outputs are available from these circuits as noted on the schematic.