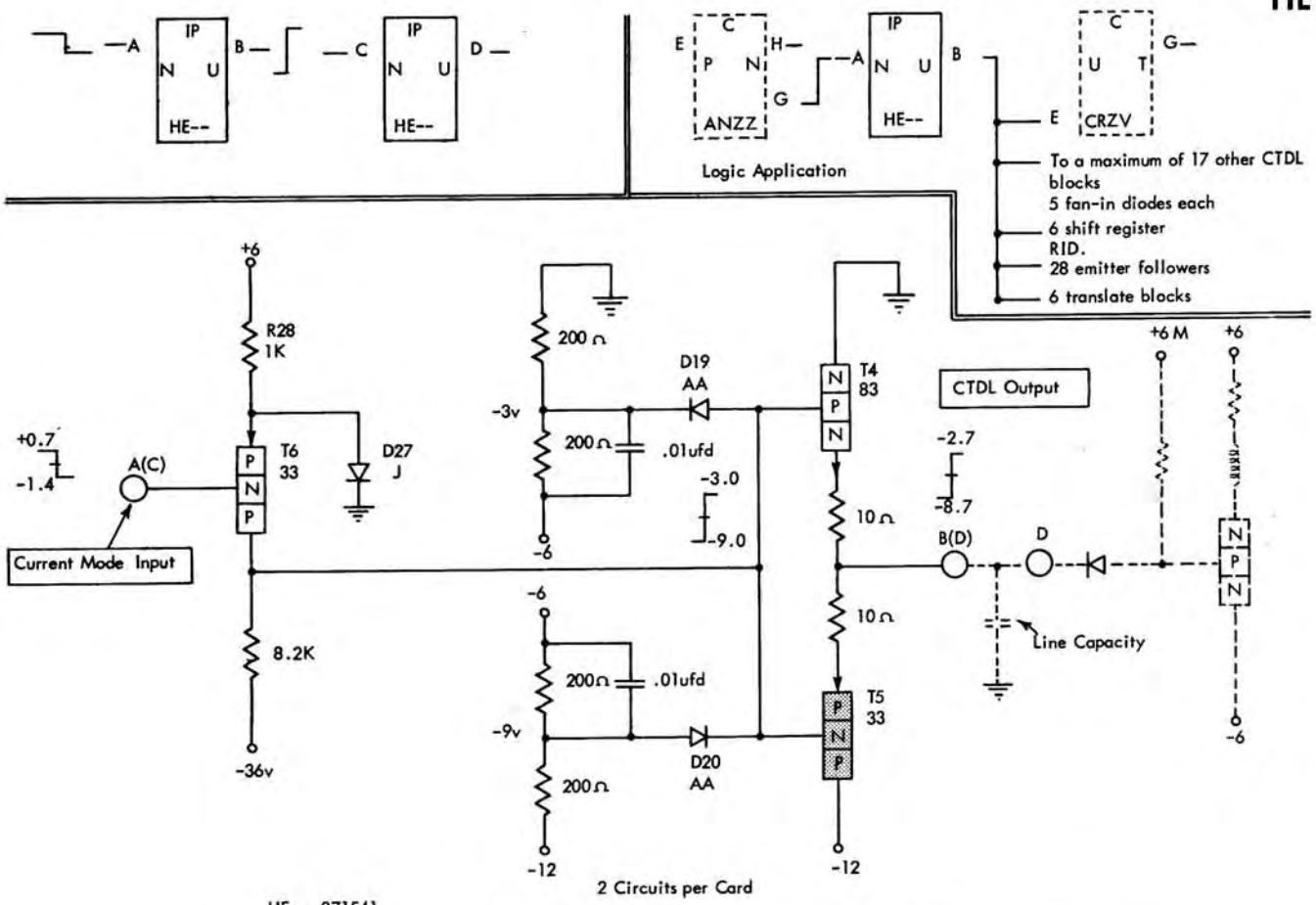

HE-- 371541

Input Level		Output Level		Delays (usec)			
Min.	Max.	Min.	Max.		Load	2 RID	10 CTDL Blocks
+0.4 to -0.4	+1.1 to -2.5	-5.3 to -7.4	-3.6 to -9.6	Turn On	Min.	.13	.18
					Max.	.15	.28
				Turn Off	Min.	.15	.14
					Max.	.26	.23

CM-to-CTDL Power Inverter

The HE- - card consists of two power inverter circuits used for converting a current mode N line input to an out-of-phase CTDL U line output. Each circuit on the card has a basic inverter driving into complementary emitter followers. The input circuit is normally driven by the current mode timing rings, or logic circuits. The power inverter output drives into CTDL U type blocks or into shift register read-in drivers.

Circuit Description

Assume that the power inverter is driving into the CTDL block as shown above. T5 is on; T4 and T6 are off. The emitter of T6 is at 0v. With a +N input at pin A, T6 is held reverse-biased off. Its collector output is set by electron flow from the −36v collector supply to the complementary emitter follower bases, where it is clamped to near −9.0v by D20 to the divider network. T5 continues to conduct, giving an output at pin B of −8.7v.

When a −N input appears at pin A, T6 is forward-biased on. The collector voltage of T6 attempts to go to 0v but is clamped to −3v by D19. T4 becomes forward-biased on and T5 is reverse-biased off. Conduction through T4 quickly charges the line capacity and increases the output at pin B to −2.7v.

The complementary emitter follower action permits the circuit to charge and discharge large capacitive loads, which results in an output signal with sharp rise and fall characteristics.

Application

Maximum DC loading for this power inverter circuit is noted in the logic application shown above.