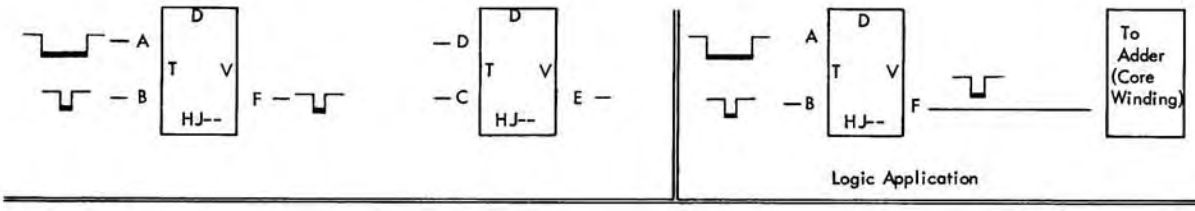

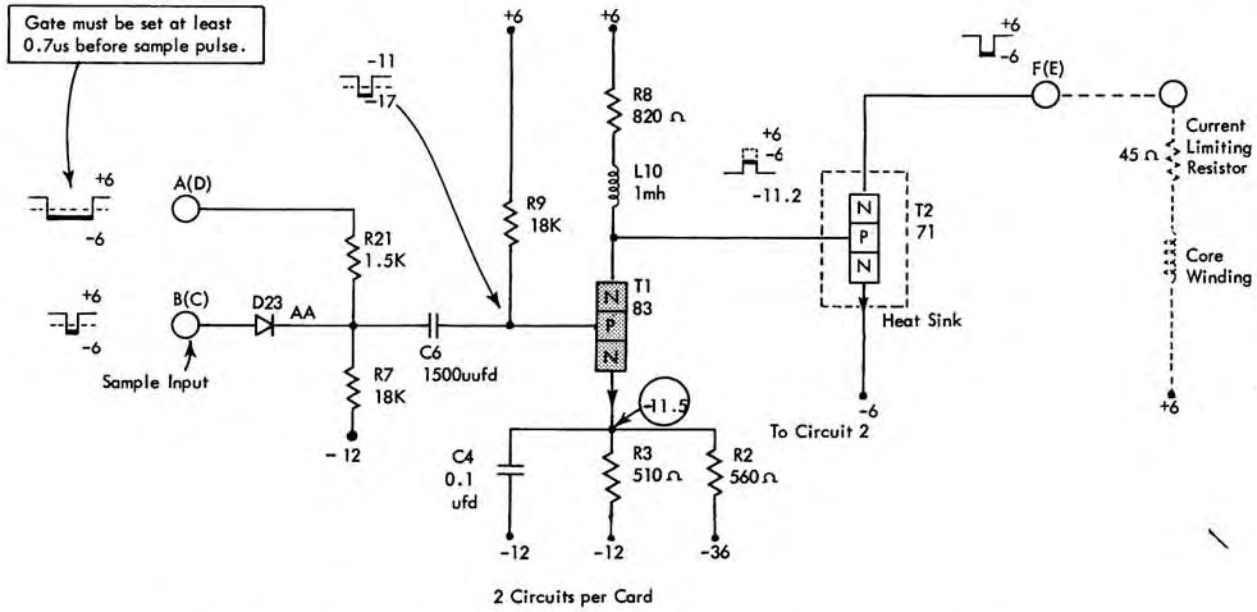

HJ-- 371530

Input Levels		Output Levels		Delays		(usec)	On Output Current
Min.	Max.	Min	Max.		Per	Circuit	
+3 / -3	+6 / -6	5.76 / -5.76	6.24 / -6.24	Turn On	Min.	0.17	250 ma
					Max.	0.30	
				Turn Off	Min.	0.12	
					Max.	0.23	

Core Adder Driver

The HJ - - card consists of two core adder driver circuits that provide the necessary current to the core adder and core translator input windings. Each circuit is controlled by a T line signal and T line gate inputs. Both the gate and signal inputs must be down to have output current flow.

Circuit Description

In a quiescent state, T1 is forward-biased on and its collector voltage is near −11.2v. T2 is reverse-biased off and no current flows in the core windings. When the gate is up, conduction through R7 and R21 to the +6v level prevents the −T input signal from turning off T1. T1 continues to conduct and keeps its collector voltage near −11.2v. T2 is reverse-biased off and no output current flows through the core winding.

Coincidence of a −T gate and a −T signal level permits the base of T1 to be reverse-biased off. The voltage at the collector of T1 increases toward +6v, but clamps at −5.7v when T2 becomes forward-biased and conducts. T2 provides up to 300ma to the core adder or translator input winding.

The RC time of C6 and R9 is such that the signal coupled to the base of T1 is of essentially the same duration as the signal input pulse. The divider network of R2 and R3 sets the emitter voltage of the input transistors on circuits 1 and 2 to −11.5v. For reliable operation, the gate input must be set at least 0.7 microseconds before the sample pulse is applied.