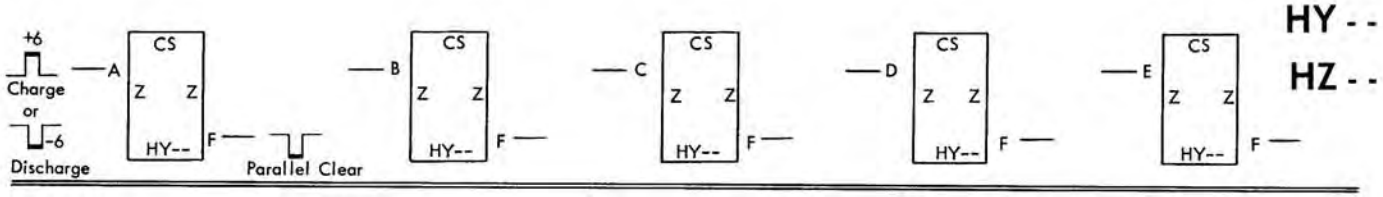

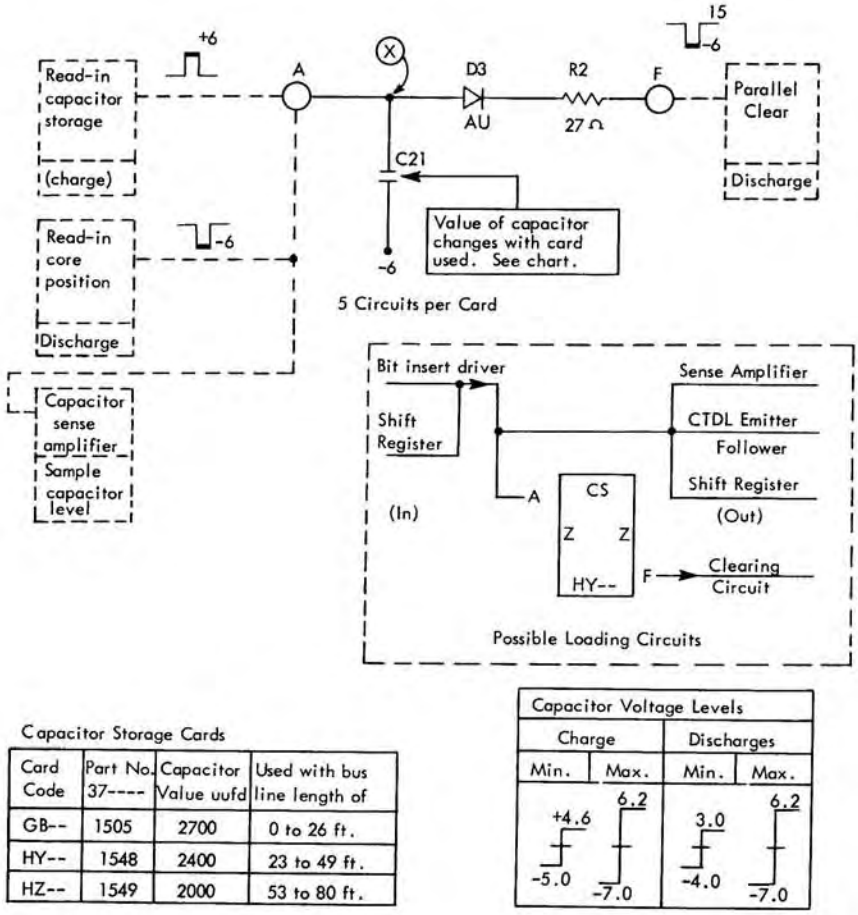

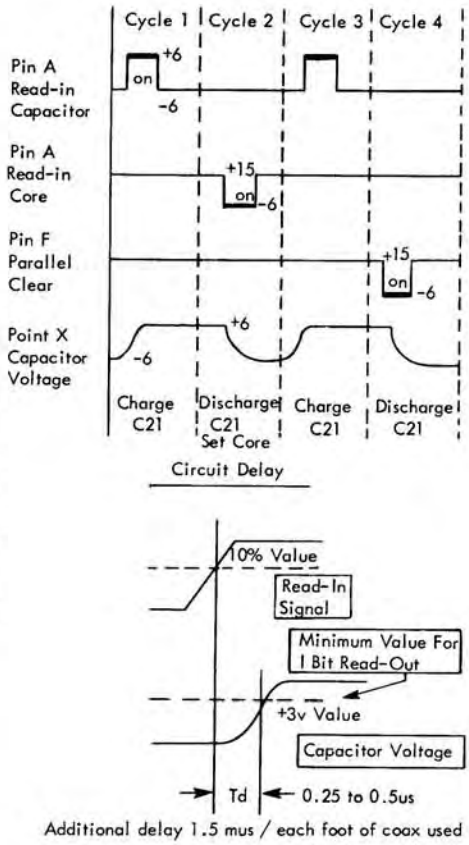

Capacitor Storage Cards

Card Code	Part No. 37----	Capacitor Value uufd	Used with bus line length of
GB--	1505	2700	0 to 26 ft.
HY--	1548	2400	23 to 49 ft.
HZ--	1549	2000	53 to 80 ft.

Capacitor Voltage Levels

Charge		Discharges	
Min.	Max.	Min.	Max.
+4.6 to -5.0	6.2 to -7.0	3.0 to -4.0	6.2 to -7.0

Capacitor Storage

The HY - - card consists of five capacitor storage circuits, each capable of storing one binary bit by virtue of its two possible states, charged and discharged. The input to the capacitor storage card is from the parallel output of a core register position or from a bit insert driver. Capacitor storage status is detected by sensing the voltage level on the capacitor. Capacitor storage outputs drive core register bit positions, sense amplifiers or CTDL emitter followers. The capacitor charge is removed by a special clearing circuit tied to pin F.

Circuit Description

Assume the capacitor storage circuit is connected as shown and that the capacitor is discharged (−6v).

Cycle 1, Charge Capacitor. When the read-in capacitor circuit at pin A is at +6v, conduction from point X to the read-in capacitor storage circuits charges the capacitor to +6v.

Cycle 2, Discharge Capacitor. The capacitor charge remains at +6v and may be sampled for system use until the read-in core driver circuit drops the voltage at pin A to −6v. The capacitor discharges to this value and the resulting discharge current is enough to set a magnetic core of a shift register position to the 1 state.

Cycle 3, Charge Capacitor. Again the read-in capacitor storage circuit causes the voltage at pin A to increase to +6v, and charges the capacitor to this value.

Cycle 4, Discharge Capacitor. To prevent the capacitor from being charged by the Ico of the shift register transistors, the parallel clear line is gated on at the end of each read-out cycle to discharge the capacitor. Discharge current from pin F, R2, and the forward-biased D3 reduces the voltage at point X to −6v. D3 provides isolation to the parallel clear circuit when it is off (+15v).

Application

In the 7070 system these cards serve as bus capacitors for transferring information bits to and from memory or core registers. The pulse duration of the capacitor charge varies from 2 to 4 microseconds depending on circuit use. The storage cards are used in both 4 and 6 microsecond transfer cycles. To compensate for line capacitance, three capacitor cards are available for driving different length bus lines.