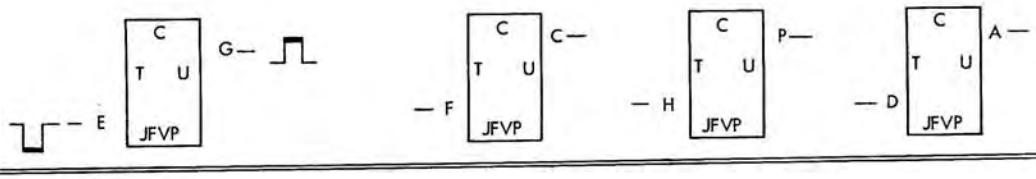

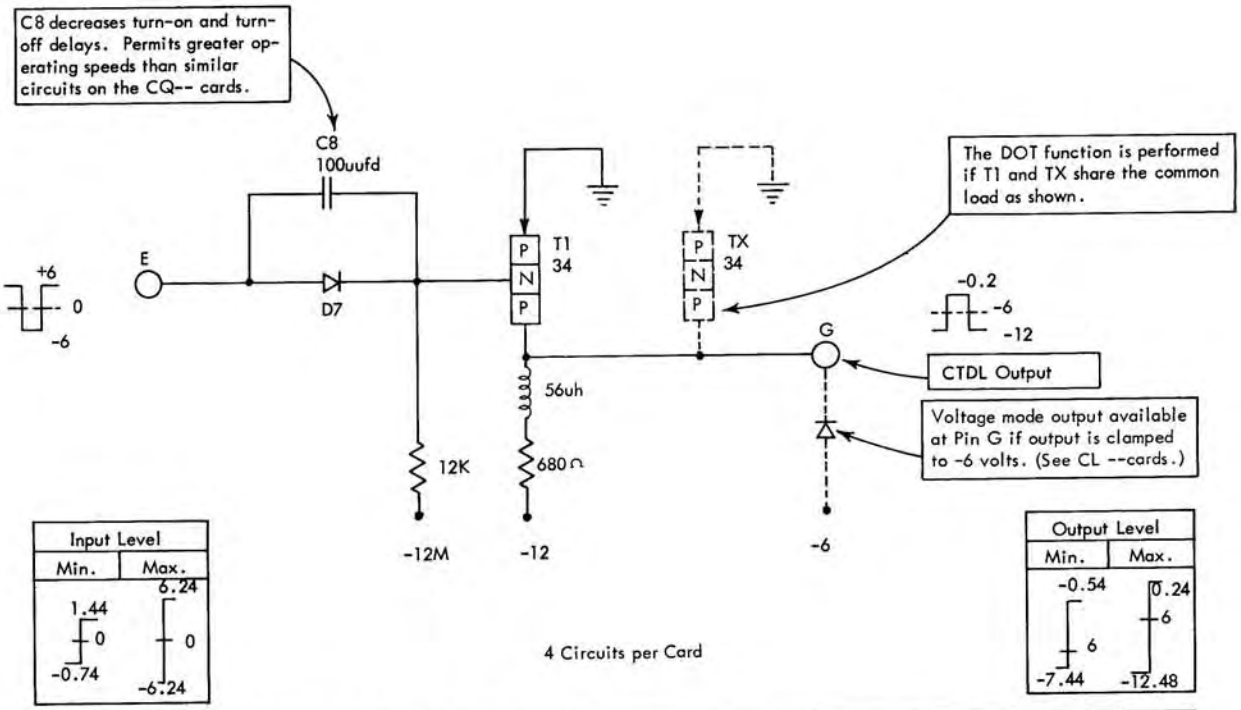

Card Code	Part No 37----	Extender Input Circuit	CM Output Circuit	Collector Loading Circuit 1	2	3	4	Delays	Per	Basic Block (usec)	Par'lel C'lector	CM Base	Diode Input	100 uufd	Circuit Use
JFVP	1576	No	No	Yes	Yes	Yes	Yes	Turn On	Min.	.075	.00	.00	.00	.02	+C
JFVN	1577	No	No	Yes	Yes	No	No		Max.	.22	.007	.015	.02	.05	+CO
JFVA	1578	No	No	Yes	No	No	No	Turn Off	Min.	.100	.004	.005	.00	.03	
JF--	1579	No	No	No	No	No	No		Max.	.150	.01	.02	.005	.06	

CTDL High Speed T-to-U Converter

The JFVP card consists of four one-way PNP logic circuits. Each circuit on the card converts a T input to an out-of-phase U output. This card is similar to the standard CTDL one-way block except that the input circuit is changed to permit a higher speed of operation. In this group of cards the base resistor is reduced in value and a capacitor is placed across the input diode. These changes reduce the turn-on and turn-off times of the transistor and result in faster switching action in the output circuit.

Circuit Description

Assume a starting condition of T1 off as shown above. When the input signal decreases suddenly to −6v, a surge of current flows through the 12K resistor and C8. This current flow quickly drops the base voltage of T1 below ground and drives T1 into saturation. The output at pin G nears 0v minus the slight drop across T1. After the initial surge of current charges C8 and forward-biases T1 on, normal diode action insures that T1 remains in saturation for the remainder of the −T input signal.

Similarly, when the input returns to +6v, current flow through the 12K resistor and C8 quickly raises the base level above ground potential and removes the minority carriers from the base region. T1 is biased-off and provides a −U output level at pin G. Conduction through D7 holds T1 off for the remainder of the +T input signal.

Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading is noted above for the different cap connections in this group of cards. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT function is accomplished by connecting similar output pins together to share a common collector load. CTDL and voltage-mode outputs are available from these circuits as noted on the schematic.