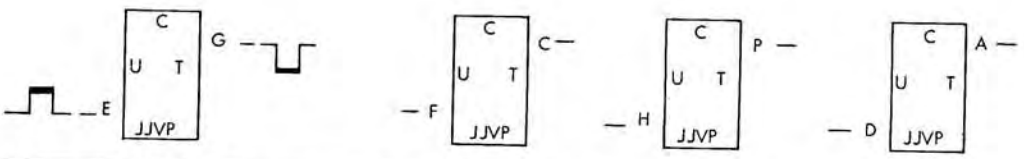

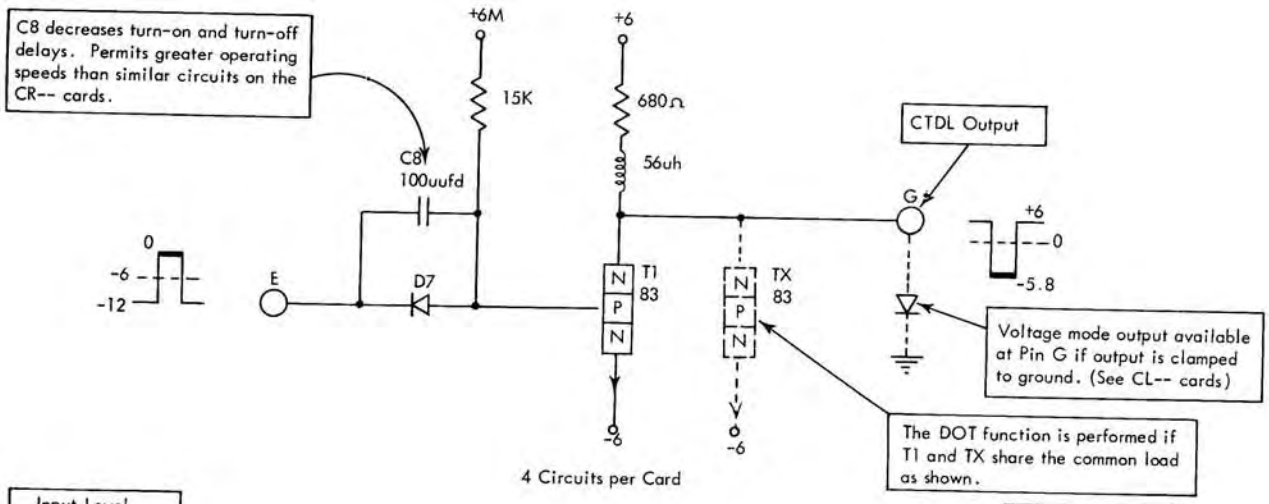

4 Circuits per Card

Input Level	
Min.	Max.
-5.3	0.24
-7.4	-6
	-12.48

Output Levels	
Min.	Max.
1.44	6.3
-5.5	-6.3

Card Code	Part No 37----	Extender Input Circuit	CM Output Circuit	Collector Loading Ckt 1	Ckt 2	Ckt 3	Ckt 4	Delays	Per	(usec) Basic Block	Par'lel C'lector	CM Base	Diode Input	100 uufd	Circuit Use
JJVP	1587	No	No	Yes	Yes	Yes	Yes	Turn On	Min.	.09	.00	.00	.00	.02	+C
JJVN	1588	No	No.	Yes	Yes	No	No		Max.	.19	.007	.02	.02	.03	+CO
JJVA	1589	No	No	Yes	No	No	No	Turn Off	Min.	.015	.004	.005	.000	.03	
JJ--	1590	No	No	No	No	No	No		Max.	.09	.01	.02	.005	.06	

CTDL High Speed U-to-T Converter

The JJVP card consists of four one-way NPN logic circuits. Each circuit on the card converts a U input to an out-of-phase T output. This card is similar to the standard CTDL one-way block except that the input circuit is changed to permit higher speeds of operation. A capacitor is placed across the input diode to reduce the turn-on and turn-off times of the transistor, which results in faster switching action in the output circuit.

Circuit Description

Assume a starting condition of T1 off as shown above. When the input signal increases suddenly to 0v, a surge of current flows through C8 and quickly forward-biases the base of T1. T1 is driven into saturation and provides a −T output at pin G. After the initial surge of current charges C8 and forward-biases T1 on, normal diode action insures that T1 remains in saturation for the remainder of the +U input signal.

Similarly, when the input signal returns to −12v, current flow through C8 quickly drops the base level below −6v and rapidly removes the minority carriers from the base region. T1 is biased off and provides a +T output level at pin G. Conduction through D7 holds T1 off for the remainder of the −U input signal.

Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Application

Internal collector loading for the different cap connections in this group of cards is noted on the circuit diagram. External collector loading is required for the unloaded circuits. Logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT function is accomplished by connecting similar output pins together to share a common collector load. CTDL and voltage-mode outputs are available from these circuits as noted on the schematic.