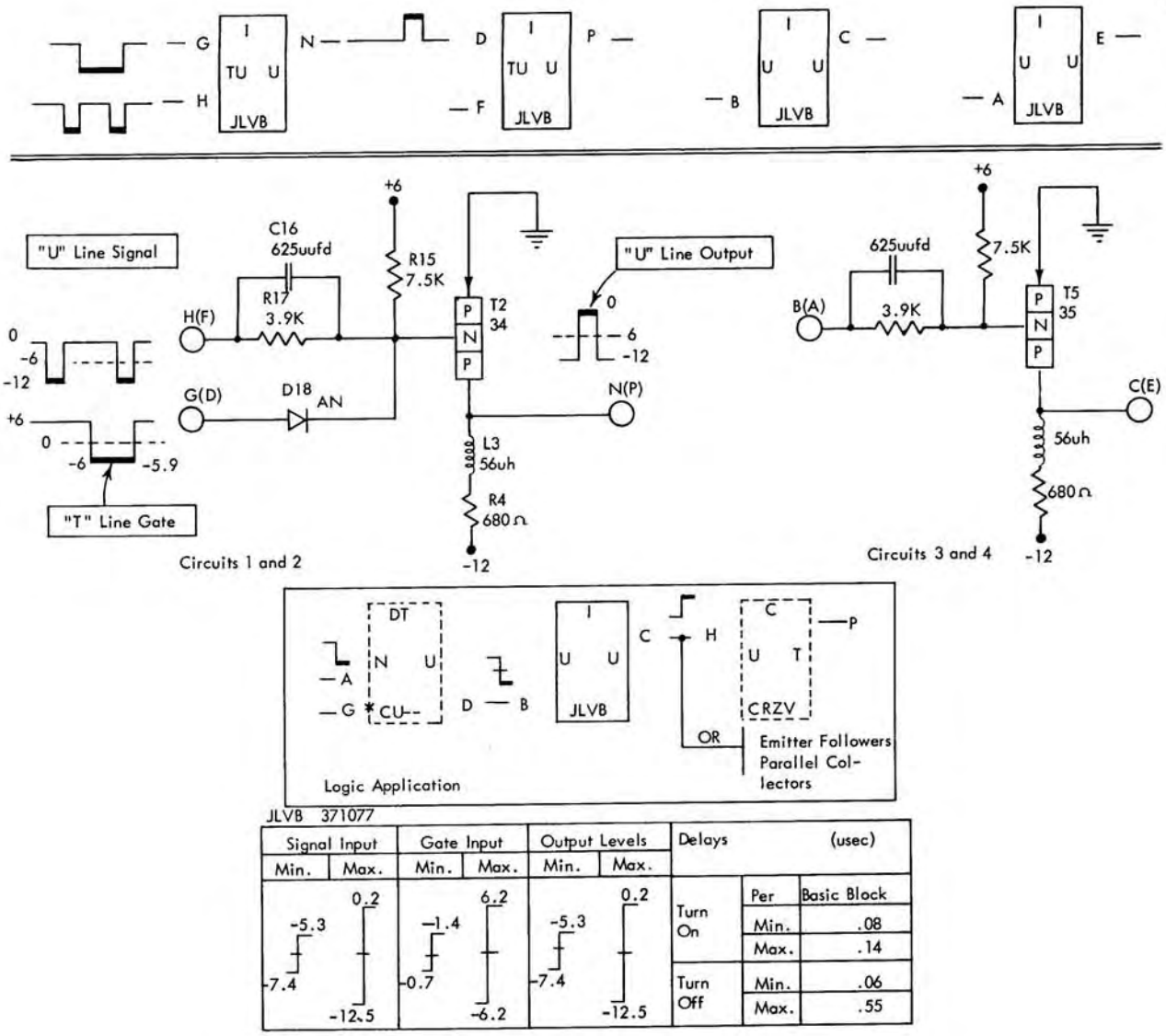

JLVB 371077

Signal Input		Gate Input		Output Levels		Delays		(usec)
Min.	Max.	Min.	Max.	Min.	Max.			
-5.3 / -7.4	0.2 / -12.5	-1.4 / -0.7	6.2 / -6.2	-5.3 / -7.4	0.2 / -12.5			
						Turn On	Per	Basic Block
							Min.	.08
							Max.	.14
						Turn Off	Min.	.06
							Max.	.55

CTDL PNP Logic Inverter

This card consists of four PNP non-translating inverter circuits used for current amplification. All circuits function as CTDL U line inverters and provide the drive to P type logic blocks. Circuits 1 and 2 have an additional T line gate input that controls the transistor bias level for these circuits. When both inputs are used, the gate and signal inputs must be down for transistor turn-on. All circuits have internal collector loads.

Circuit Description (Circuits 1 and 2)

Gate Up — Signal Up. When the gate is up at pin G and the signal input is up at pin H, conduction through R17 to D18 and R15 sets the base of T2 to approximately +6v. T2 is reverse-biased off and the output at pin N is at −12v.

Gate Down — Signal Up. With a −T gate input at pin G and a +U signal input at pin H, conduction through R17 and R15 sets the base of T2 near +2.1v. T2 remains reverse-biased off and the output at pin N stays at −12v.

Gate Down — Signal Down. When a −T gate input is applied to pin G and a −U input is applied to pin H, conduction through R17 and R15 to D18 forward-biases T2 on. The output at pin N increases rapidly to ground potential, and current flows in an external load. C16 improves the shape of the output signal.

Application

These circuits provide inversion of a U line input signal, and drive into CTDL logic blocks or emitter followers.