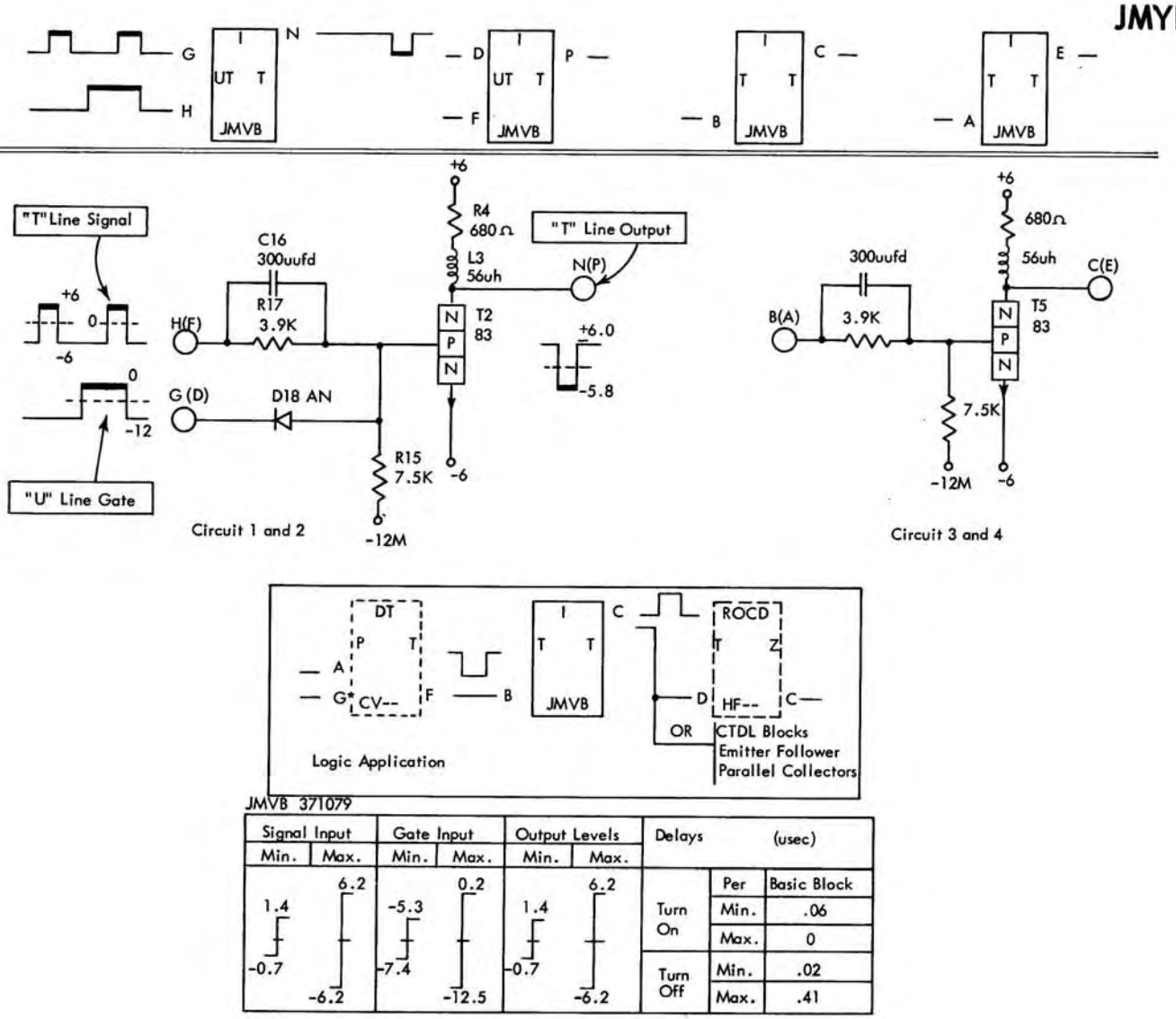

JMVB 371079

Signal Input		Gate Input		Output Levels		Delays		(usec)
Min.	Max.	Min.	Max.	Min.	Max.			
1.4 to -0.7	6.2 to -6.2	-5.3 to -7.4	0.2 to -12.5	1.4 to -0.7	6.2 to -6.2		Per	Basic Block
						Turn On	Min.	.06
							Max.	0
						Turn Off	Min.	.02
							Max.	.41

CTDL NPN Logic Inverter

This card consists of four NPN non-translating inverter circuits used for current amplification. All circuits function as CTDL T line inverters and provide the drive to N type logic blocks. Circuits 1 and 2 also have an additional U line gate input which controls the transistor bias level for these circuits. When both inputs are used, both the gate and signal inputs must be up for transistor turn-on.

Circuit Description (Circuits 1 and 2)

Gate Down — Signal Up. When the gate is down at pin G and the signal input is up at pin H, conduction through D18 and R15 to R17 and the +6v signal sets the base of T2 near −12v. T2 is reverse-biased off and the output at pin N is +6v.

Gate Up — Signal Down. If the gate is up at pin G and the signal input is down at pin B, conduction from −12v through R15 and R17 to pin H sets the base of T2 near −8.5v. The transistor remains reverse-biased and the CTDL output at pin N stays at +6v.

Gate Up — Signal Up. When the gate input at pin G is up, and the signal input at pin H is up, conduction through D18 and R17 and R15 and R17 to the +6v signal input increases the base voltage above −6v and drives T2 into saturation. The output voltage at pin N is approximately −6v (minus the small drop across the forward-biased transistor). C16 improves the shape of the output signal. The peaking coil L3 provides a high impedance when T2 is first turned on, and improves the leading edge of the output wave.

Application

These circuits provide inversion of a T line input signal and drive CTDL logic blocks or emitter followers.