CTDL Trigger 2

The JZ - - card consists of a CTDL trigger circuit designed for use in clock and ring circuits and as a single bit memory device. The bistable circuit consists of two inverters and two emitter followers operated at a frequency near 250kc. A positive CTDL signal applied to the AC set and gate inputs or to the extender inputs control the triggering action. Both in-phase and out-of-phase outputs are available from this card.

This card differs from the CTDL trigger circuit on the CW - - card in that extender inputs are provided on this card in place of the DC set inputs. A special trigger extender card (JN - -) is available that permits additional inputs to control the trigger.

AC Set Input and Gate. When the trigger is used as a single-bit memory device, both the signal input and the gate input are driven by CTDL U lines. The gate sets the reference threshold for the AC set input and must be conditioned 3.75μs before the set signal is applied. If the gate is up, a positive U line shift having a minimum pulse duration of 0.5μs is required to flip the trigger.

Circuit Description

Assume a starting condition of T4 and T2 conducting and T3 and T1 off. When coincidence of +U levels occurs at pin A and pin B, the base of T4 becomes more positive than the emitter (ground potential). T4 becomes reverse-biased off and causes its collector voltage to drop to −12v.

This negative swing is coupled through C23 to forward-bias T3 on and also to T2 to decrease the conduction through the emitter follower. Conduction through T3 causes its collector voltage to increase to 0v. This positive swing is coupled to T4 by C24 (keeping it cut off) and also to the base of T1. T1 becomes more forward-biased and conducts harder, causing the emitter follower output (pin P) to increase to +2.7v. This up level is latched back through D12 to keep T4 cut off. If +U levels are now applied to pins D and C, the trigger is flipped to its original state. The positive level at the input pins cuts off T3, causing its collector to drop to −12v.

This negative shift is coupled through C24 to forward-bias T4, and drive it into conduction. The collector voltage of T4 goes to 0v and allows the emitter follower T2 to conduct more. The positive shift at the collector of T4 is also coupled through C23 to keep T3 cut off. The emitter follower output at pin N (+2.7v) is latched back through D11 to keep T3 cut off.

The turn-on and turn-off delays are a function of circuit loading and are noted above for nominal conditions. Overall trigger delays in flipping from state to state average from 0.12μs to 0.45μs.

Application

This circuit is used mainly in ring applications (e.g., digit and word rings) to provide output pulses of a specific duration. It is also used as a storage device in a binary operation. Various logic block configurations for the trigger are illustrated above.