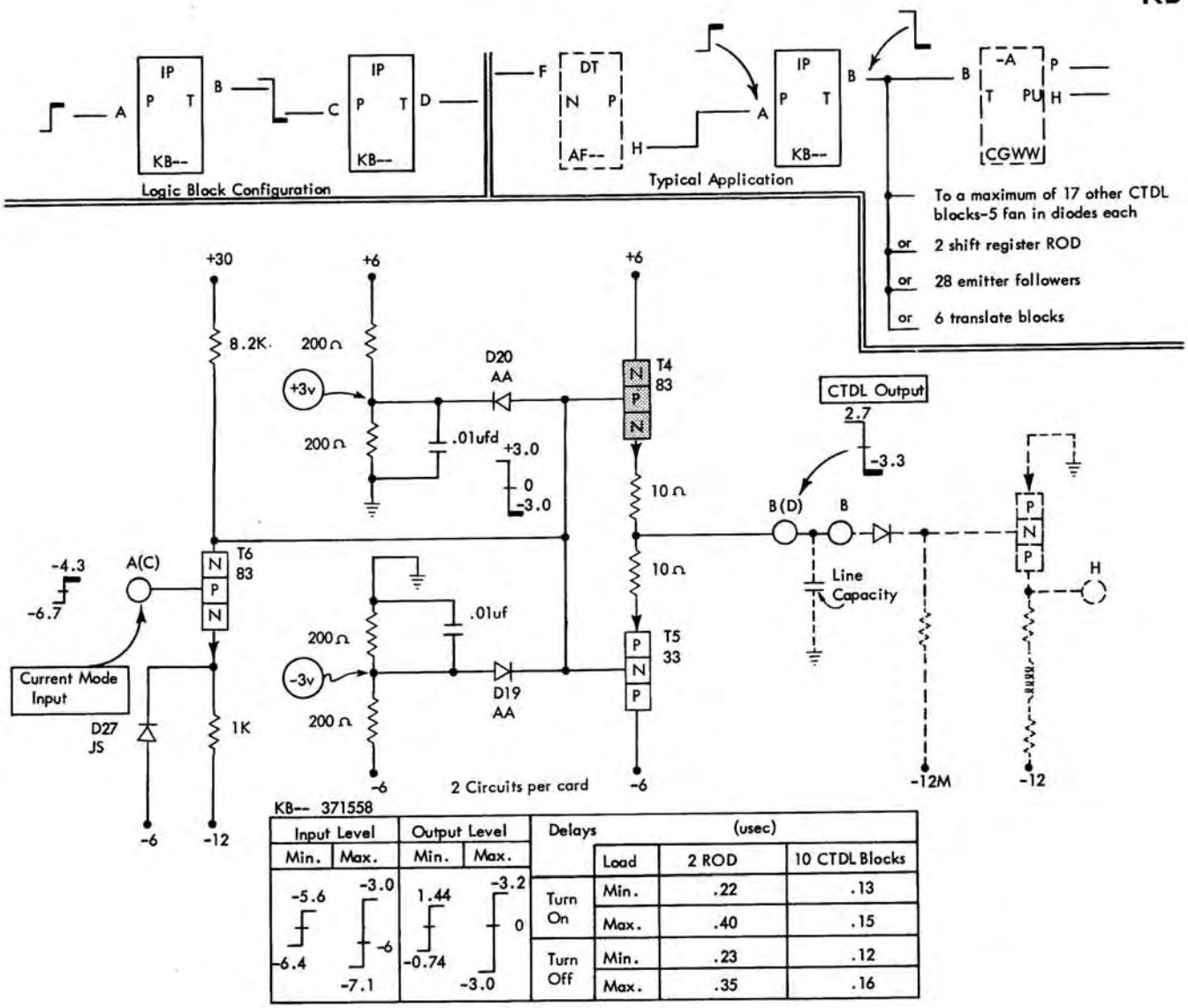

KB-- 371558

Input Level		Output Level		Delays (usec)			
Min.	Max.	Min.	Max.		Load	2 ROD	10 CTDL Blocks
-5.6 to -6.4	-3.0 to -7.1	1.44 to -0.74	-3.2 to -3.0	Turn On	Min.	.22	.13
					Max.	.40	.15
				Turn Off	Min.	.23	.12
					Max.	.35	.16

CM to CTDL Power Inverter

This card consists of two power inverter circuits used for powering and converting a current mode P line input to an out-of-phase CTDL T line output. Each circuit on the card has an inverter controlling a complementary emitter follower. The input circuit is normally driven by current mode timing rings, or from current mode outputs available from CTDL circuitry. The power inverter outputs drive CTDL N blocks and shift register read-out drivers.

Circuit Description

Assume that the power inverter is driving into the CTDL block as shown above. T4 is on and T5 and T6 are off. The emitter of T6 is at −6v. With a −P input at pin A, T6 is reverse-biased off. The collector voltage of T6 attempts to go to +30v but is clamped to near +3v by conduction from the divider network and D20, to the 8.2K resistor to +30v. T4 is forward-biased on and T5 is reverse-biased off. Line capacity quickly charges and the output at pin B is a usable +T output.

When a +P input appears at pin A, T6 is forward-biased on. The collector voltage of T6 attempts to go to −6v but is clamped to near −3v by conduction through D19 to the divider network. T4 is reverse-biased off and T5 is forward-biased on. Conduction through T5 quickly discharges the line capacity and decreases the voltage at pin B to −3.3v. Use of the complementary emitter followers results in an output signal having sharp rise and fall characteristics.

Application

Maximum DC loading for this power inverter circuit is noted in the logic application illustrated above.