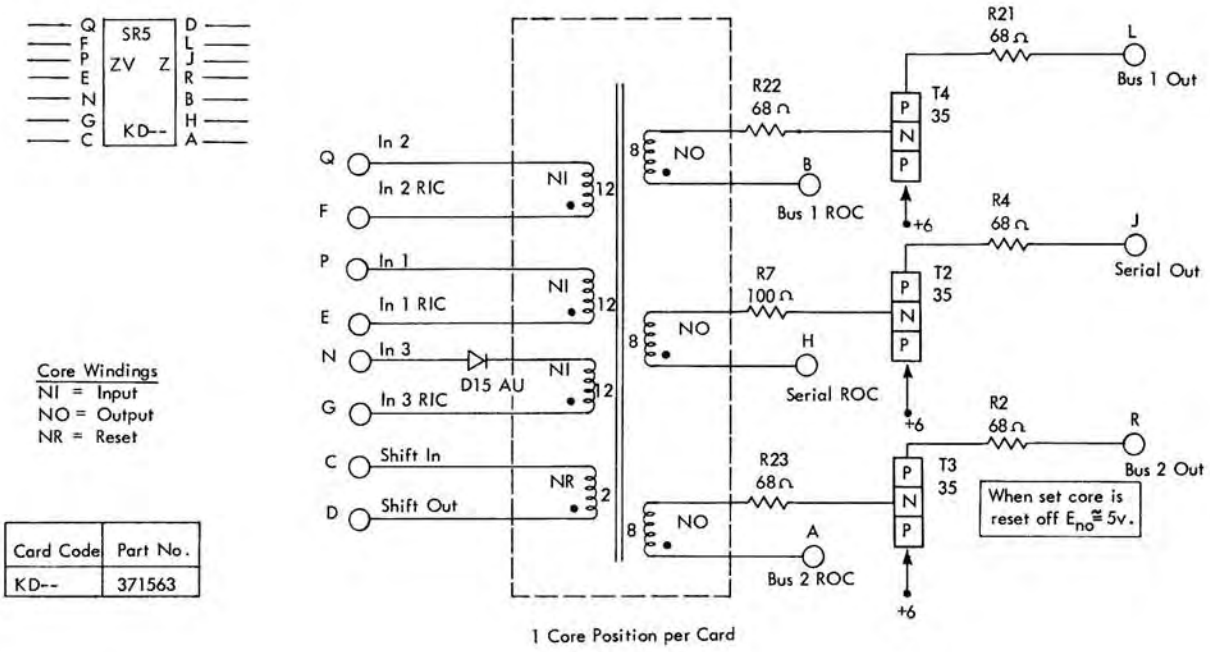

Magnetic Core Shift Register (Significant Digit Detection)

The KD - - card consists of a single magnetic core position used in circuits to detect the high-order significant digit of a magnetic core shift register. Each core position contains three input windings, three output windings, and a reset or read-out winding. The isolation diodes are removed from input windings 1 and 2, to permit their use in the significant digit detection circuits. Magnetic core operation is essentially the same as for other shift register cards. The three outputs from this card are used to charge capacitor storage networks.

Circuit Description

Figure KD-1 illustrates a typical application of the SR5 card. The figure shows several SR5 cards combined to form a circuit that determines which position of an N digit shift register contains the high-order significant digit. The digits from the capacitor bus lines are coded in the 2-of-5 bit code, with a zero being represented by a 1 bit and a 2 bit. Sampling the 0, 3 and 6 bit bus lines by an OR circuit indicates the presence of a significant digit and causes current to flow in the set input windings.

Assume the conditions as noted in Figure KD-1. The high-order digit position (N) of the shift register driving into the OR circuit contains a zero (1 bit and 2 bit only) and the remaining lower-order digit positions all contain significant digits (indicated by the plus entries to their respective OR circuits). When the outputs of the OR circuits are sampled, the sense amplifiers for the N-1, N-2 and N-3 digit positions are gated on and 30ma of current flows through their respective SR5 set windings (Ns) and the inhibit windings (Ni) to the −12v supply. The core for the high-order digit position (N) is not set, because a significant digit was not sensed and current does not flow through its set winding. The core for the N-1 digit position is set on because 30ma of current flows through its set winding (no current through its inhibit winding). Although the N-2 and N-3 cores also have 30ma through their set windings, they also have current flow through their respective inhibit windings that prevents the cores from being set on.

Thus, only the core for the N-1 position is set on and indicates that this is the high-order significant digit in the register. On the next read-out cycle, all the cores are reset off by a constant current pulse from a read-out driver and approximately 5v is induced in the output winding (No) of the N-1 digit core position, because of the switching of its core. At this time, the read-out control driver (ROCD) would be on (+6.5v), and would permit the transistor (TX) to be forward-biased on. This provides sufficient current to charge the bus capacitor storage for that position.

The total current through any one inhibit winding is a function of the number of significant digits sensed in the higher order positions.

For additional information on basic magnetic core shift register operation, refer to the FX - - card.