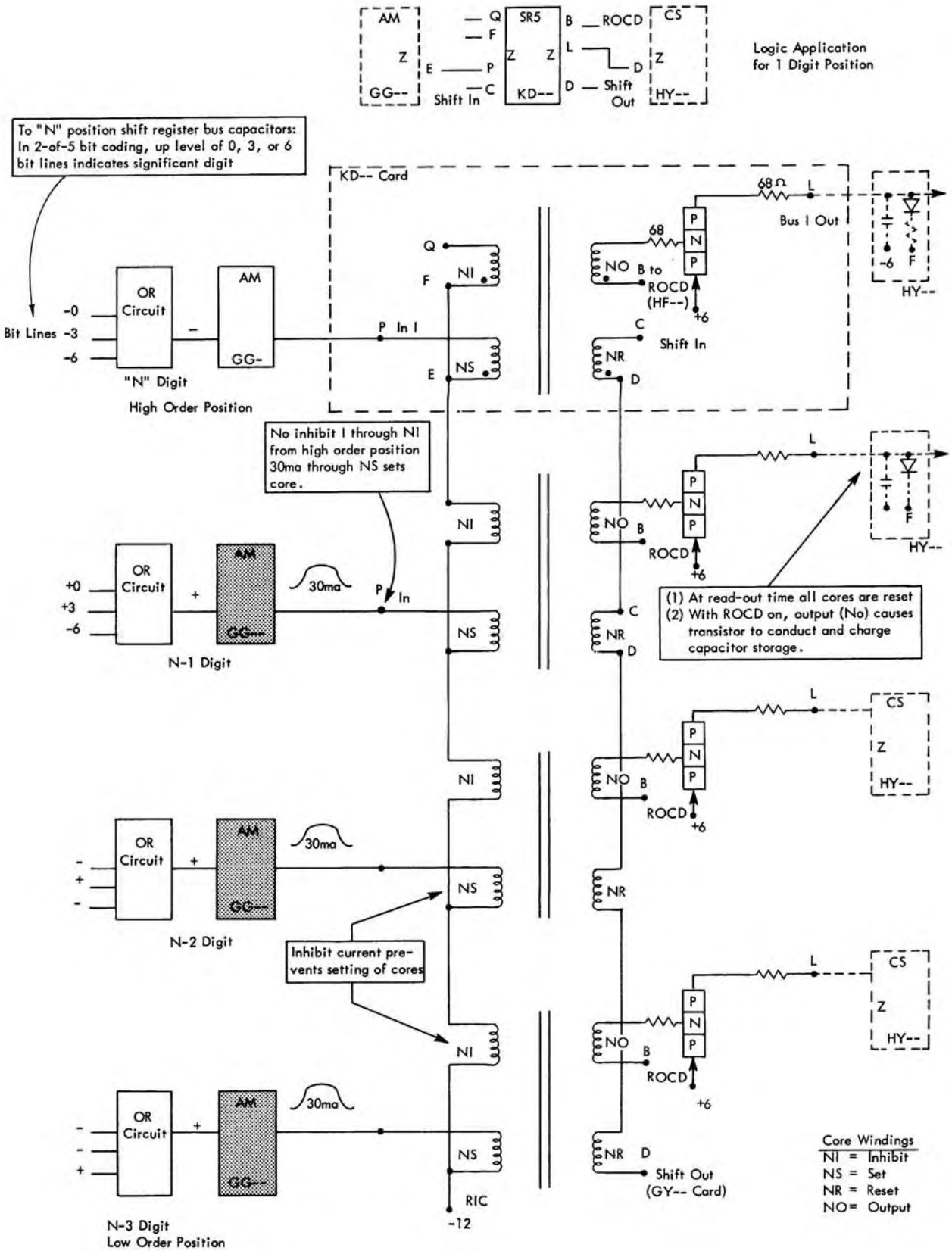
AM
Z
GG--
E
P
C
Shift In
Q
F
SR5
Z
Z
KD--
B
ROCD
L
D
Shift Out
CS
Z
HY--
Logic Application for 1 Digit Position
To "N" position shift register bus capacitors: In 2-of-5 bit coding, up level of 0, 3, or 6 bit lines indicates significant digit
KD-- Card
Bit Lines -0 -3 -6
OR Circuit
AM
GG-
"N" Digit
High Order Position
P In 1
NI
NS
Q
F
E
68 Ω
L
Bus 1 Out
68
P
N
P
NO
B to ROCD (HF--)
+6
C
Shift In
NR
D
-6
F
HY--
No inhibit I through NI from high order position 30ma through NS sets core.
+0 +3 -6
+
30ma
P In
N-1 Digit
ROCD
(1) At read-out time all cores are reset
(2) With ROCD on, output (No) causes transistor to conduct and charge capacitor storage.
- + -
N-2 Digit
Inhibit current prevents setting of cores
- - +
N-3 Digit
Low Order Position
RIC
-12
Shift Out
(GY-- Card)
Core Windings
NI = Inhibit
NS = Set
NR = Reset
NO = Output