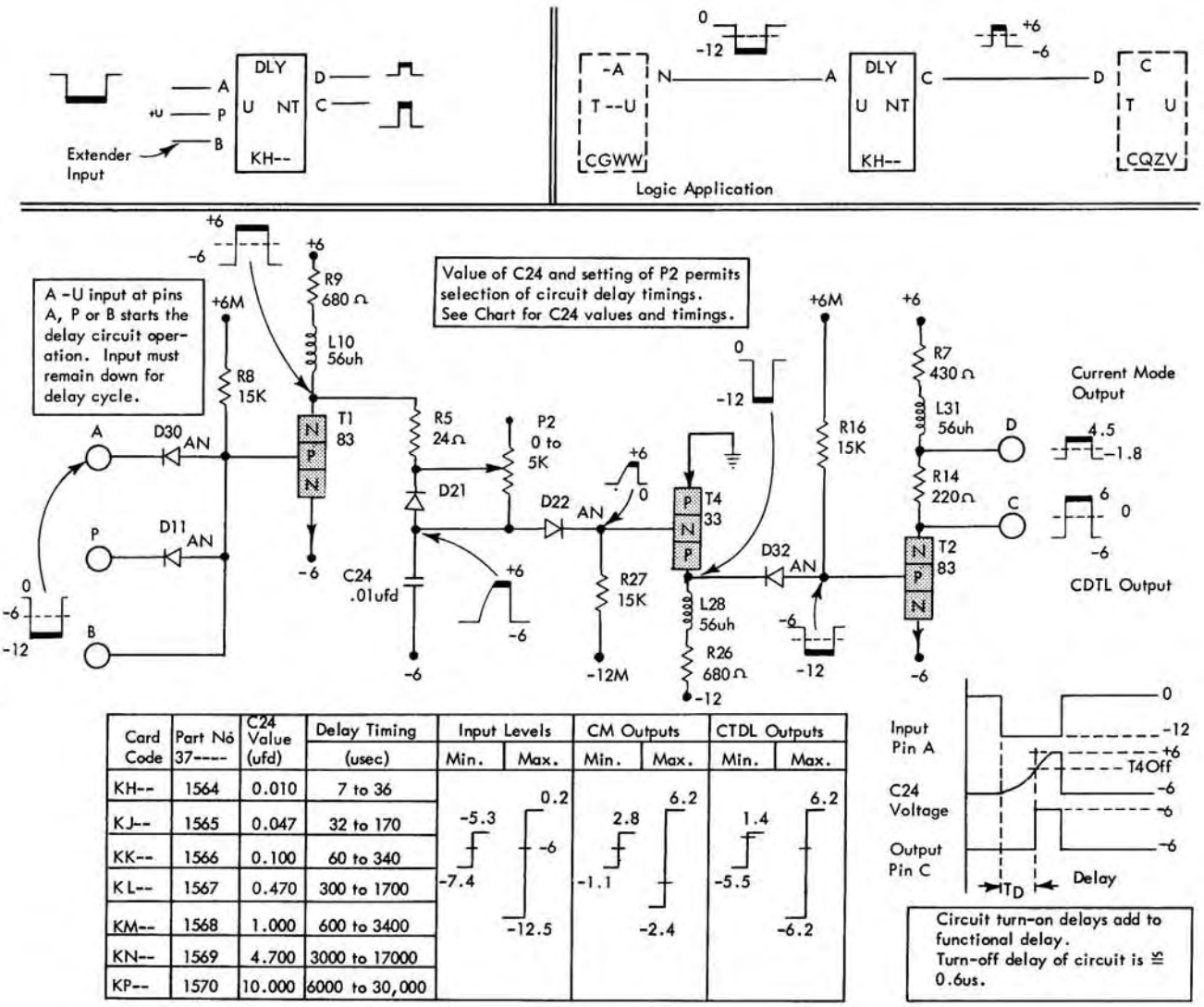

Card Code	Part Nó 37----	C24 Value (ufd)	Delay Timing (usec)	Input Levels Min.	Input Levels Max.	CM Outputs Min.	CM Outputs Max.	CTDL Outputs Min.	CTDL Outputs Max.
KH--	1564	0.010	7 to 36	-5.3 / -7.4	0.2 / -6 / -12.5	2.8 / -1.1	6.2 / -2.4	1.4 / -5.5	6.2 / -6.2
KJ--	1565	0.047	32 to 170						
KK--	1566	0.100	60 to 340						
KL--	1567	0.470	300 to 1700						
KM--	1568	1.000	600 to 3400						
KN--	1569	4.700	3000 to 17000						
KP--	1570	10.000	6000 to 30,000						

CTDL Delay Circuit

The KH - - delay card provides an output pulse 7 to 36μs after the start of the input pulse. There is one delay circuit on each card that is controlled by an RC network. A 5K potentiometer is varied to obtain a desired delay within the 7 to 36μs range.

A −U level at any of the input pins starts the delay timing and provides out-of-phase N and T line outputs. The output duration is a function of the input signal and the circuit variables. This circuit is self-recycling, but requires a definite off period to insure the discharging of the timing capacitor (C24).

Circuit Description

Assume all inputs are in the up level, and T1, T4 and T2 are forward-biased and conducting. The CTDL output at pin C is near the −6v emitter potential of T2. C24, the timing capacitor, is discharged to −6v through T1, R5, and the forward-biased D21.

When a −U level appears at pin A, T1 is reverse-biased off. The collector voltage of T1 increases to +6v. D21 is no longer forward-biased, so C24 must now charge through the 5K potentiometer, R2 and R5 toward the +6v collector supply. T4 remains in conduction until the charge on C24 is positive enough to reverse-bias T4. When T4 is turned off, its collector voltage drops to −12v and cuts off T2. The collector output of T2 increases to +6v. This +T output (pin C) remains up until all inputs again are at the +U level. The RC charging time thus controls the cut-off time of T4 and delays the start of the positive output swing for the desired time interval.

Repetition Rate

The input must remain in the up level long enough to insure that the timing capacitor is fully discharged (approximately 1.3 to 1.6 times the circuit delay).

Application

Seven CTDL delay cards with various capacitor sizes provide continuous delay timings (with good overlap) from 7.0 to 30,000μs. The range of delay timings available and the value of C24 used for the various delay cards are noted in the chart.