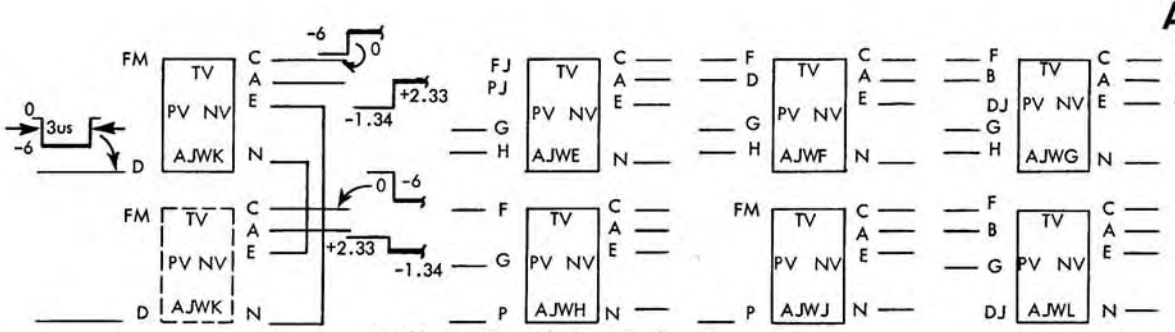
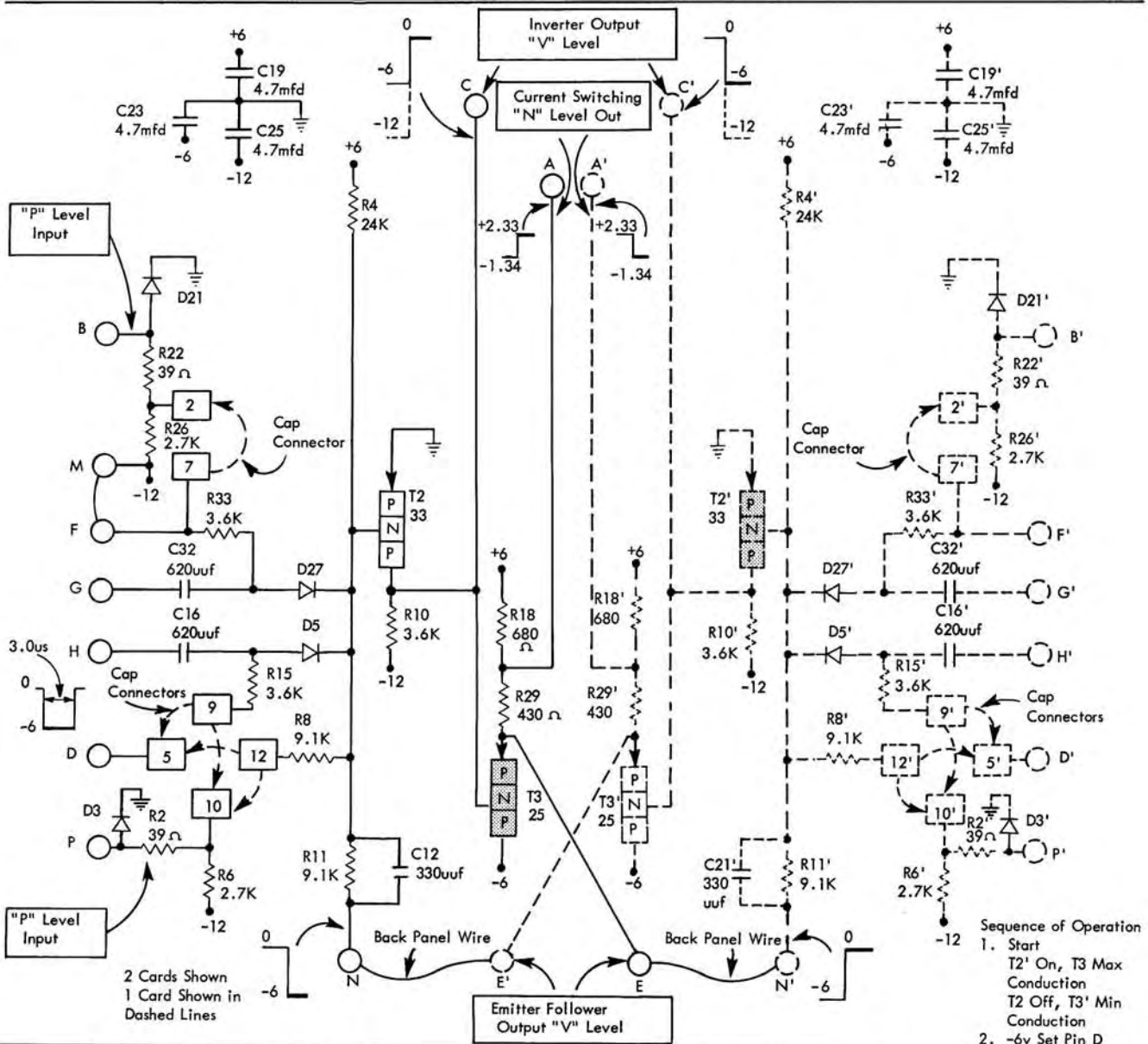
AJWE
WF
WG
WH
WJ
WK
WL



Possible Cap Cuts and Circuit Configurations



Sequence of Operation

1. Start
   T2' On, T3 Max Conduction
   T2 Off, T3' Min Conduction
2. -6v Set Pin D
   T2 On, T3 Min Conduction
   T2' Off, T3' Max Conduction

Input						Levels		Output Levels					
AC Set		Gating				DC Set		Emitter Follower		Inverter		"N" Level	
Min	Max	Current Mode		Votlage Mode		Current Mode	Voltage Mode	Min	Max	Min	Max	Min	
		Min	Max	Min	Max								
2.6	Limited only by Gate Level and Reverse Bias Spec of Transistor	(ma) 4.82	7.3	+0.35 -0.2		$I_{IN} \leq$ 7.3ma $I_{IN} \geq$ 4.82 ma for set Operation	-0.2	-0.2	+0.35	-0.2	0	+2.05	
		0.186	0	-5.56	-12.48		-5.56 -12.48	-5.56	-6.24	-5.56	-6.24	-0.42	