Voltage Mode Trigger 3

The AJ-- card consists of one inverter and one emitter follower connected to form half of a voltage mode trigger. Two cards are required to form a trigger that may serve as an isolated binary bit memory or may be used in a clock or ring circuit. By use of cap cuts, the basic card may be varied to provide seven different input configurations. Each of the seven different cap cut configurations, may then be backpanel wired to provide varied input and output applications. The following data show the relationship between part number, cap cut coding, cap connections, and input configurations.

Card and Cap Type	Part Number	Cap Connection	AC Sets	Input CM Gates	Input VM Gates	Types VM DC Set	Types CM DC Set
AJWE	371424	2 to 7 9 to 10	2	2	1	0	0
AJWF	371423	5 to 9	2	0	2	0	0
AJWG	371422	2 to 7 5 to 9	2	1	2	0	0
AJWH	371421	10 to 12	1	0	1	0	1
AJWJ	371420	2 to 7 10 to 12	1	1	1	0	1
AJWK	371419	5 to 12	1	0	1	1	0
AJWL	371418	2 to 7 5 to 12	1	1	1	1	0

In-phase and out-of-phase V level and N level outputs are available from this trigger. This trigger circuit operates at a frequency near 200KC.

Binary Operation: The trigger may be operated in a binary state by connecting the gate resistors to the emitter follower output on the same side of the trigger and connecting the AC inputs together to the output of a sample pulse driver.

AC Set Input: There are two gated AC sets per state (pins G and H) and either AC set may be gated by current mode (pins B and P) or voltage mode gating (pins D and F). The AC set pulse may be either a 3v or a 6v positive shift with a minimum rise rate of 2.6v in 0.9μs and a minimum pulse duration of 0.5μs.

The following data show levels and timings for gated operation:

AC Set	VM Gating	CM Gating	Gate Condition Time	Minimum Gate Level
3v	−12.48v		7.0μs	−.5v
3v	−6.2v		5.5μs	−.5v
6v	−12.48v		4.0μs	−2.0v
6v	−6.2v		3.0μs	−2.0v
6v		6.0ma	5.0μs	4.8ma

DC Set Input: A negative signal of −5.56v minimum and −12.48v maximum applied to the VM DC set (pin D) input triggers the circuit. A current mode signal of 4.82ma minimum and 7.3ma maximum applied to the DC current mode input (pin P) also triggers the circuit. The pulse duration for voltage mode DC set is 3.0μs.

Circuit Description

Assume a starting condition of T2′ conducting, T3 in maximum conduction, T3′ in minimum conduction, and T2 off. With a 0v to −6v negative signal of at least 3.0μs duration on pin D, the base of T2 is forward-biased and goes into full conduction. The inverter output of T2 (pin C) rises from −6v to 0v. This voltage rise from −6v to 0v is fed to the base of T3, reducing its forward bias, and causing reduced current through the emitter follower T3. The reduced current through the emitter follower T3 allows its output to rise from −6v to 0v (pin E) and reverse bias T2′. T2′ is turned off because of the reverse bias, and its collector output tries to go to −12v. Because the base of the emitter follower T3′ is tied to the collector of T2′ and because the collector of T3′ is connected to −6v, the diode action between the collector and base of T3′ clamps the output of the inverter T2′ to −6v (pin C′). T3′ goes into full conduction, and because the emitter output of the emitter follower T3′ follows the base, its output (pin E′) goes from 0v to −6v. The current mode outputs (pins A and A′) follow the emitter follower outputs (pins E and E′) in proportion to the resistor divider networks and the loads that they are connected to. A negative pulse applied to pin D′ flips the trigger to its original state.

The maximum turn-on delay is 0.8μs and the minimum turn-on delay is 0.3μs. The maximum turn-off delay is 0.54μs and the minimum turn-off delay is 0.14μs.

Application

This circuit is used mainly for register and ring applications. Various logic block configurations and the seven cap cuts are shown.