The AR - - card consists of a voltage mode trigger circuit designed for use in clock and ring circuits and as an isolated binary bit memory. The trigger circuit uses two inverters and two emitter followers and operates at a frequency near 150KC. The trigger may be connected to be operated by many input configurations. It may be operated as a binary input, a single gated AC input, a dual gated AC input, or a DC set input. Both in-phase and out-of-phase outputs are available from this card.

Binary Operation: The trigger may be connected for binary operation (gated or not gated) by connecting one of the gate resistors to the emitter follower output on the same side of the trigger. The other gate input may be then used as an external gate or tied to ground. The two AC inputs are connected together and driven from a sample pulse driver to form the binary operation.

AC Set Input: For gated input operation, the AC set pulse may be either a 3v or a 6v positive shift with a minimum rise rate of 2.6v in 0.9μs and a minimum up duration of 0.5μs. The following data show the input shifts and the time required to condition the gates (The gates have to be at about ground level for a 3v AC input shift to flip the trigger.).

AC Set Input	Gate 1	Gate 2	Gate Condition Time	Minimum Gate Level
3v	−12.48v	−12.48v	7.5μs	−0.5v
3v	−12.48v	GND	6.0μs	−0.5v
3v	−6.2v	−6.2v	6.0μs	−0.5v
3v	−6.2v	GND	4.5μs	−0.5v
6v	−12.48v	−12.48v	4.5μs	−2.0v
6v	−12.48v	GND	3.0μs	−2.0v
6v	−6.2v	−6.2v	3.0μs	−2.0v

DC Set Input: A signal of −5.56v (or more negative) applied to the DC set input triggers the circuit. The negative set signal may go as far negative as −12.48 volts. The down input pulse must be at least 3.0μs in duration.

Circuit Description

Assume a starting condition of T4 and T2 in full conduction, T3 at minimum conduction, and T1 off. With one gate (pin B) tied to ground (pin J) and the other gate (pin D) gated from −6v to 0v for 4.5μs before the AC input shift is applied, a positive going 3v pulse of 0.5μs is applied to the AC set input (pin C). The output of the gate at D24 causes the base of T4 to become more positive than the emitter (ground potential). T4 becomes reverse-biased off and its collector voltage tries to go to −12v. Because of the diode action between the collector and base of T3, the collector of T4 is allowed to go only to −6v (pin F). This negative −6v forward biases T3 into full conduction. The emitter of the emitter follower (T3) follows the base to −6v. The output of the emitter follower (pin E) is coupled to the base of T1 through the voltage divider R3 and R5, forward biasing T1. The conduction of T1 causes its collector (pin G) to rise from −6v to 0v. This T1 collector voltage rise to 0v is fed to the base of T2 and reduces the forward bias of T2. The reduced bias on the emitter follower (T2) reduces its conduction so that its emitter rises to 0v. The emitter output of T2 (0v) at pin H is coupled back to the base of T4 and holds reverse bias on T4, thus providing latch back to the circuit. If gating of pins L and P and an AC set pulse to pin N are applied, the trigger is flipped to its original state.

The turn-on and turn-off delays are a function of circuit loading.

Application

This circuit is used mainly for ring and register applications. Various logic block configurations for the trigger circuit are possible; some of these configurations are shown.