The AS - - card consists of a voltage mode trigger circuit designed for use in clock and ring circuits and as an isolated binary bit memory. The trigger circuit uses two inverters and two emitter followers and operates at a frequency near 150KC. The trigger may be connected to operate in many configurations. It may be operated as a binary input or AC set input. Two AC set inputs per state are available. Both in-phase and out-of-phase outputs are available from this card.

Binary Operation: The trigger may be connected for binary operation (gated or non-gated). When it is used as a non-gated trigger, the gate inputs are tied to ground, and the AC set inputs are tied together and driven by a sample pulse driver.

AC Set Input: For gated input operation, the AC set pulse may be either a 3v or a 6v positive going pulse with a minimum shift of 2.6v in 0.9μs and a minimum up duration of 0.5μs. Because there are two AC set gates per state in this circuit, the trigger can be driven from either gate input as gated or non-gated, or the gates may be connected together and operated as a single AC set input. The following data show levels and timings for gated AC input operation:

AC Set Input	Gate 1	Gate 2	Gate Condition Time	Minimum Gate Level
3v	−12.48v	GND	6.0μs	−0.5v
3v	−6.2v	GND	4.5μs	−0.5v
6v	−12.48v	GND	3.0μs	−2.0v

Circuit Description

Assume a starting condition of T4 conducting, T2 in maximum conduction, T1 off and T3 in minimum conduction). When triggering only one capacitor input (pin C), pin D has to be gated from −6v to 0v for 4.5μs (minimum) before the positive going 3v pulse of 0.5μs is applied to the AC set input (pin C). The output of the gate at diode D24 causes the base of T4 to become more positive than the emitter (ground potential). T4 becomes reverse-biased off and its collector voltage tries to go to the −12v. Because of the diode action between the collector and base of T3, the collector of T4 is allowed to go only to −6v (pin F). This negative −6v forward biases T3 into full conduction and its emitter follows the base to −6v. The output of the emitter follower T3 (pin E) is coupled to the base of T1 by voltage divider R3 and R5 and forward biases T1 (−6v). Conduction of T1 causes its collector (pin G) to rise from −6v to 0v. This 0v at the collector of T1 is fed to the base of T2 and reduces the forward bias of T2. The reduced forward bias of T2 reduces its conduction so that the emitter of T2 (pin H) rises to 0v. The 0v output of T2 is coupled back to the base of T4 and holds reverse biasing on T4, providing latch back to the circuit. If gating of pins L or P and an AC set to pins N or R is applied, the trigger is flipped to its original state.

AC set inputs A and R and their respective gates B and P provide additional possible means of flipping the trigger. By use of both AC sets per state (pins A and C and pins R and N), bidirectional counters and registers can be constructed.

Turn-on and turn-off delays are a function of circuit loading.

Application

This circuit is used mainly for counter and register applications. Various logic block configurations for the trigger circuit are possible and some of the configurations are shown.