Gated Sample Pulse Driver 2

This family of sample pulse drivers (DSP) is used to drive voltage mode triggers 1, 2 and 3. An output repetition frequency, independent of circuit loading, is obtained from each card in this group. Circuit operation is similar for all the cards and the different cap connections permit flexibility of application. These pulse generators are driven by either voltage mode or current mode circuits and have various collector loadings which produce either a 6v or a 3v output shift.

The circuits function as single-shot oscillators and provide about a 1μs output pulse regardless of the input signal duration. A gated, positive signal to the voltage mode inputs or a +N level at the current mode input starts the single-shot action.

Circuit Description

Cap connections on the schematic are those found on the AYWS card. The normal status of this circuit is: T4 conducting, T1 partially conducting, T2 cut off, and output pin G at −9.5v. There are two inputs, both conditioned by a single gate that must be up to 0v before either input can operate the circuit. The output expected is a 3v positive, 1μs pulse regardless of input duration in excess of 1μs.

With the input gate (pin C) at 0v for more than 7.5μs, a positive shift at input pin B cuts off T4. The attempt to reduce current through the 200μh inductance is resisted with a strong negative potential at the normally positive end of the coil. This negative spike passes through the 390$\mu\mu$f capacitor and drives T1 base negative. T1 emitter seeks to follow T1 base but is clamped by T2 emitter-base diode action. T1 base is, in turn, clamped by T1 emitter. T2 in full conduction brings output pin G up to −6v. This level is maintained while the 390$\mu\mu$f capacitor charges to −5.2v, through T1 emitter-base junction and T2 emitter-base junction. T2 is reverse-biased off when its base rises more positive than its emitter (−6.0v) and drops the output at pin G back to −9.5v.

The input signal must extend beyond the 1μs period to allow the circuit to time out. The 390$\mu\mu$f capacitor discharges through the 2K resistor.

Because of the large voltage developed by the collapsing field of the 200μh inductor, capacitors (C5, C30) are provided to short to ground any interference that might be introduced onto the −6v and −12v supply leads. The diode in parallel with the inductor prevents oscillation or ringing in the coil and speeds circuit recovery.

Other cap connections use the current mode input (pin A), which requires a current input; circuit operation is the same.

Application

The internal collector loading and input coupling network used are noted in the chart for the card code and cap connections. External collector loading is required for the unloaded circuits. Input and output waveform data are also given in the chart.

Gating: The gate input (pin C) is normally driven by CTDL, CTRL, or voltage mode trigger circuits that provide the required voltage levels. When the gate is used with the AC set 1 input, it must be conditioned 7.5μs before the set pulse is applied. When the gate is used with AC set 2 input, it must be conditioned 5.0μs before the set 2 pulse is applied.

Driving Capabilities: The 3v pulse from the DSP can drive 25 triggers (Voltage Mode Trigger 1 or 2) at a repetition rate of 150KC. The 6v pulse from the DSP can drive 25 type 3 triggers. A typical logic application is noted on the schematic.