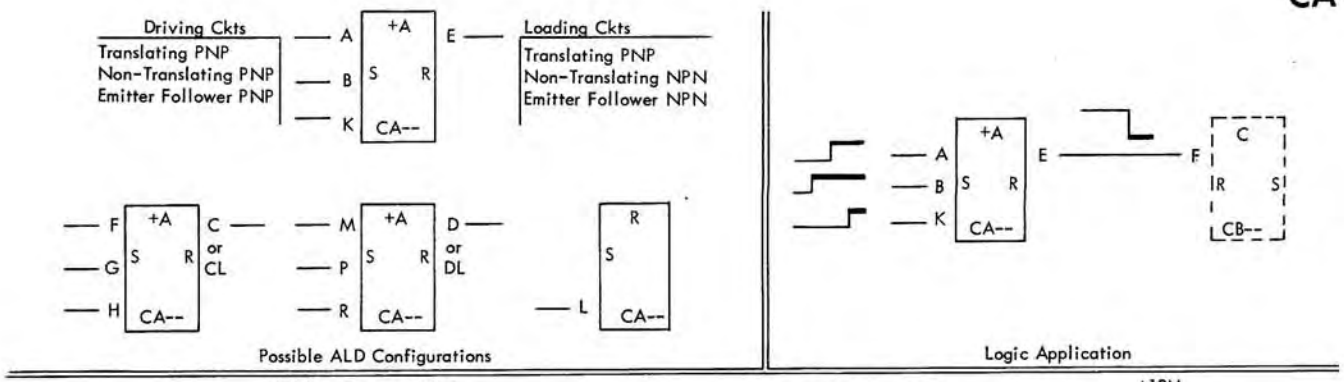

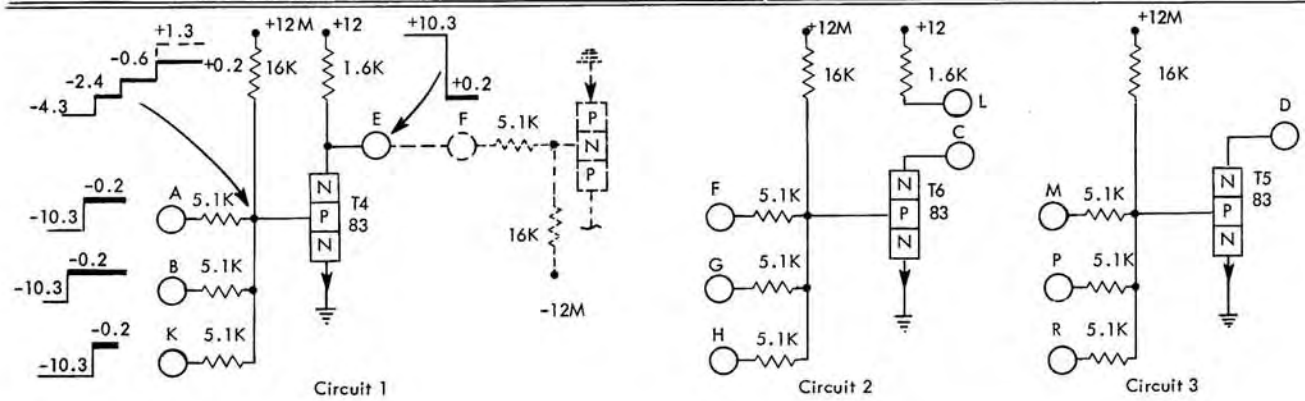

CA-- 371026

Input Levels		Output Levels		Delays (usec)						Circuit Use
Min	Max	Min	Max	Measurements	Per		Block	Additional Load	Additional Input	100 uufd	
-0.2 / -5.56	+0.35 / -12.48	+5.56 / +0.2	+12.48 / -0.35	Input, GND, -0.6, -5.25, +5.25, +0.6, GND, T_{on}, T_{off}, Output	Turn On (T_{On})	Min	+0.34	-0.06	-0.04	+0.3	+A +AO +CO +TCO +TAO +TC -O -OA -CA
						Max	+1.35	0	+0.23	+0.15	
					Turn Off $T_{(off)}$	Min	+0.26	-0.02	-0.09	+0.09	
						Max	+2.26	+0.5	-0.03	+0.18	

CTRL Three-way NPN Translating Circuits

The CA - - card consists of 3 three-way NPN translating circuits used for repowering and level setting of CTRL signals. Each circuit on the card performs a basic logical function (+A, −O, C) and inverts an S input level to an R output level. The logical function is performed by the input resistor network, and the invert function is accomplished by the common emitter transistor configuration. Collector loading differs for each circuit and permits flexibility in driving external loads and for accomplishing the DOT functions.

In the +AND, invert logic application illustrated, a −R output is obtained only when all the inputs are up (+S).

Circuit Description (Circuit 1)

The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their levels. Input levels may vary at their low levels, but all will reach ground potential (+S) when up. A −S level at any input holds the base of T4 below the emitter voltage and keeps the transistor off, causing a +R output to exist at pin E. The exact output level at pin E is dependent on the circuit loading. A typical loading circuit, indicated by the dashed lines, is tied to the output.

When all the inputs used are at the +S level, current flow into the divider network to the +12M supply raises the base voltage of T4 above ground potential. T4 is forward-biased into saturation and drops the output at pin E to the −R level.

Circuit delays are summarized in the chart for circuit and loading conditions. The delays are measured from the time the input signal reaches the circuit switching threshold until the output signal reaches the switching threshold of the loading stage.

Application

Possible logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The DOT functions are accomplished by having similar output levels share a common collector load. This sharing of a collector load provides a second level of logic in the circuits. For example, output pins D and E are back-panel wired together to perform the +AO function. These circuits can also be combined with other CTRL logic circuits to make up trigger and latch configurations. Possible driving and loading circuits are also indicated with the ALD representations.