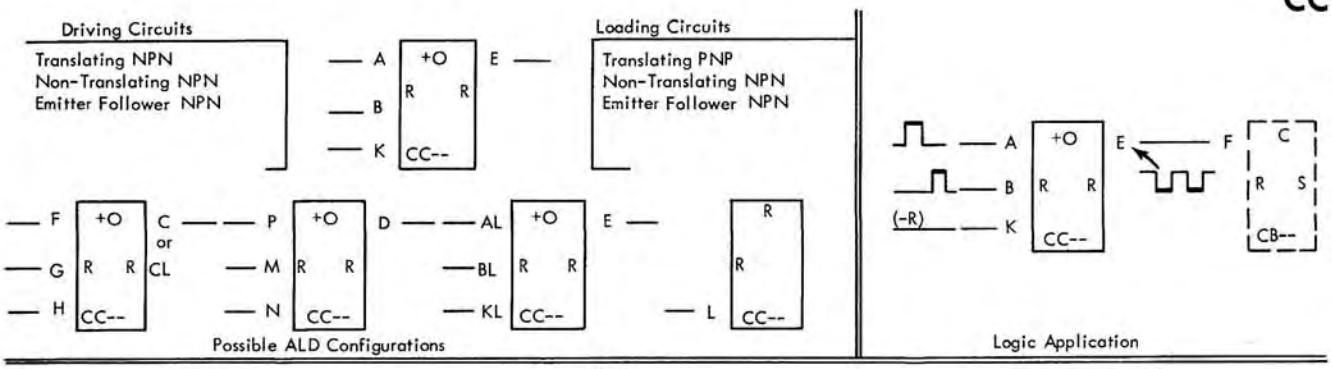

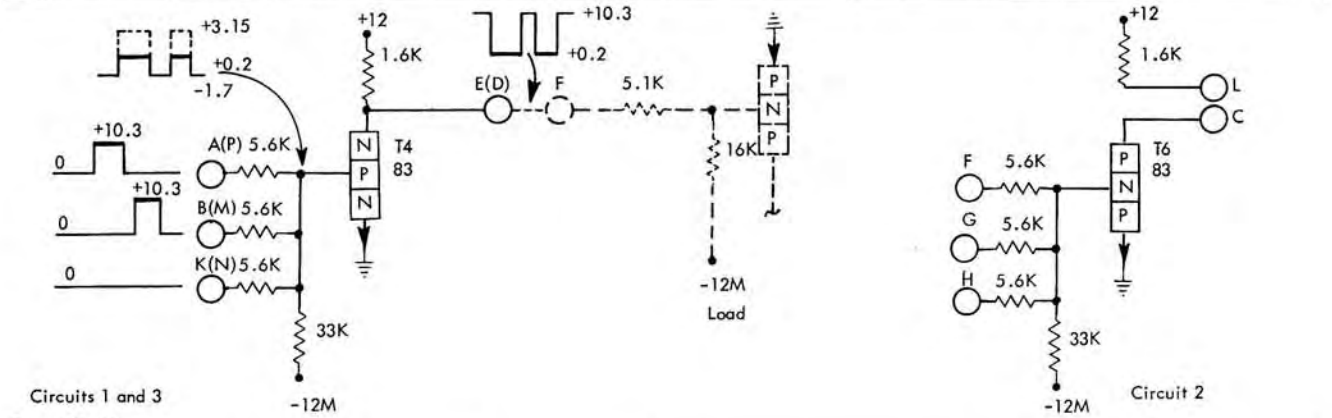

CC-- 371028

Input Levels		Output Levels		Delays (usec)						Circuit Use
Min.	Max	Min	Max	Measurement	Per		Block	Load	Ad'tional Input	100 uufd	
+0.2	+5.56	+0.2	+5.56	Turn On (T_{On})	Min		+0.26	-0.03	-0.01	+0.01	E +O +I +IO +TO +TIO +TOO -A -IA -AO
-0.35	+12.48	-0.35	+12.48		Max		+0.84	-0.02	+0.2	+0.14	
				Turn Off (T_{Off})	Min		+0.6	+0.03	-0.12	+0.01	
					Max		+2.8	+0.06	-0.04	+0.18	

CTRL Three-way NPN Non-translating Circuits (Inverter)

The CC - - card consists of 3 three-way NPN non-translating circuits used for repowering and level setting of CTRL signals. This circuit is sometimes called the NOR circuit. Each circuit on the card performs a basic logical function (+O, −A, I) and inverts the R input signal. The logical function is performed by the input resistor network and the invert function is accomplished by the common emitter transistor configuration. Collector loading for circuit 2 differs from that of circuits 1 and 3 and permits flexibility in driving external loads and for accomplishing the DOT functions. In the +OR logic application illustrated, a −R output is obtained whenever a +R level occurs at any of the input pins.

Circuit Description (Circuit 1)

The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their level. Input levels may vary at their high levels (+R), but all will reach ground potential at the −R level. When −R levels exist at all the input pins, T4 base is at −0.7v. The transistor is held reverse-biased off as its emitter is connected to ground. Current flow from the load network through the 1.6K collector resistor to the +12v supply sets the off level at 10.3v.

Increasing any input to the +R level causes T4 base to rise toward +3.15v. T4 becomes forward-biased and clamps the base at +0.2v. Saturation current flows through the transistor and quickly drops the output to the −R level (+0.2v). Coincidence of more than one +R level at the inputs drives the transistor further into saturation and increases the turn-off delay of the circuit.

Circuit delays are summarized in the chart. The delays are measured from the time the input reaches the circuit switching threshold until the output reaches the switching threshold of the loading stage.

Application

Possible logical functions of these circuits are indicated in the Circuit Use chart. DOT'ing the collectors (sharing of a common collector load by similar outputs) does not perform another level of logic, but merely increases the number of inputs. These inverter circuits are also combined with other CTRL logic circuits to make up trigger and latch configurations. Possible driving and loading circuits are indicated with the ALD representations.