

The CFYA card consists of four one-way NPN emitter follower circuits. Each circuit serves as a non-translating current amplifier that drives additional logic or branching circuits. Emitter followers also serve as buffers to match impedances or provide isolation. A slight DC voltage shift results between the input and output voltage signals. Card and circuit design permit many variations in input and output loading connections of these emitter followers. A typical circuit application, input and output type loading, and some of the possible ALD block configurations are shown above.

Circuit Description

Assume circuit 1 has the input and output loading indicated by the dash-line circuitry.

With tx1 on, T5 base is at about +0.2v and T5 is in partial conduction. Most of the current from the load and the 2.2K resistor flows through the low resistance inductor into the transistor. T5 base emitter drop (0.2v to 0.4v) gives a slight voltage shift between the input and output signals. A -R output exists at pin G and reverse biases tx2 off.

When tx1 turns off, its collector voltage rises toward +12v and increases the forward-bias on T5. Current through T5 starts to increase, but is momentarily resisted by the inductor. The voltage drop developed across the parallel LR network holds the output positive until the

counter-EMF is overcome. Then, the output increases sharply to the +R level and the transistor is in full conduction. Additional current flow into the load network forward-biases tx2 on.

The circuit is returned to its original status by a -R level to T5. The drop to the former -R level is similarly resisted by the inductor and again a sharp shift results.

Because of the relatively low impedance offered by the emitter follower, the output level is little affected by the output loading (within limits). The 300 ohm collector resistor limits the power dissipation across T5. The 0.01 μ fd capacitor filters to ground any oscillation or ringing that might be introduced onto the +12v line by the coil. Because the emitter followers are normally driven by CTRL logic or inverter circuits, the delays given in the chart are the total delays encountered through the driving circuit and the emitter follower.

Application

The logical functions performed by these circuits are indicated in the Circuit Use chart. Back panel wiring permits additional flexibility. For example, the NOR functions are accomplished by connecting similar output pins together to share a common emitter load. Wiring of an input pin to pin D allows the DE to be driven from an unloaded logic circuit.