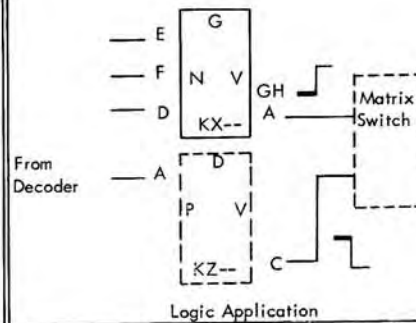
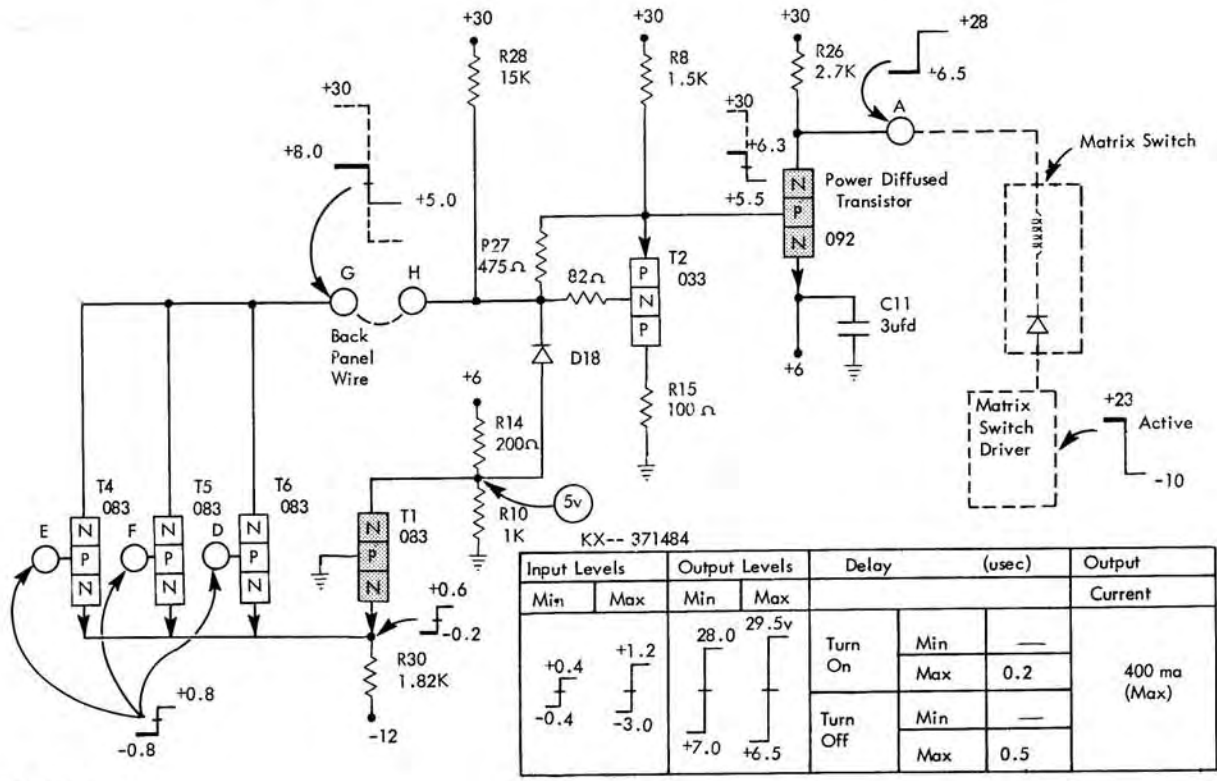


ADL Configuration



Logic Application



Input Levels		Output Levels		Delay (usec)		Output
Min	Max	Min	Max			Current
+0.4	+1.2	28.0	29.5v	Turn On	Min	—
-0.4	-3.0	+7.0	+6.5		Max	0.2
				Turn Off	Min	—
					Max	0.5

**Power Gate**

The power gate circuit on the KX--card is used in conjunction with the matrix switch driver card (KZ--) for correct addressing of the X and Y drive lines in core storage operation. This circuit is made up of a basic - AND circuit, a modified emitter follower and a power diffused junction inverter. Coincidence of -N levels at all the inputs is required for the circuit to be active. When the circuit is active, the power gate output is at +6.5v and allows a large current to flow in a selected primary winding of a matrix switch. Selection of a particular primary winding is accomplished by activating its matrix switch driver (+23v). When the power gate is inactive, only the small back-current flows through the matrix switch windings.

**Circuit Description**

**Active Status:** With a -N input at pins E, F, and D, the transistors T4, T5, and T6 are reverse-biased off and T1 is forward-biased on. The emitter voltage of T1 is clamped at -0.2v. At this time, the voltage at pin H attempts to increase toward +30v, but the power diffused transistor becomes forward-biased into conduction; base current from the power diffused transistor through R8, R27 and R28 to +30v sets the voltage at pin H near +8.0v and holds T2 reverse-biased off. Conduction through the power transistor

quickly drops the output at pin A to +6.5v and, depending on the status of the matrix switch drivers, permits current to flow in a selected primary winding.

**Inactive Status:** When a +N level is applied to pin E (or to any of the input pins), T4 becomes forward-biased on and T1 is reverse-biased off. Additional current flow through R28, R27, and R8 causes the voltage at pin H to drop 5v. T2 becomes forward-biased and conducts, quickly dropping the base voltage of the power transistor to about 5.5v. The power transistor is reverse-biased off and the output at pin A increases toward +30v. The purpose of D18 is to clamp the inactive output of T1 and T2 to the +5v set by the coupling network of R10 and R14. The clamping action limits the drive to T2 which in turn prevents the power transistor from being biased too far in the off direction. This reduces the switching time of the output seen at pin A.

**Application**

The KX--card is used in the core storage section of the IBM 7070 system. Typical circuit usage is noted above. Back panel wiring of pins G and H is required in most applications.