The MQ - - card is a clamped oscillator circuit that provides a square wave output at intervals of about 13μs. Each card configuration consists of an oscillator circuit, a feedback and clamp circuit, and an output circuit. A +S input to the feedback and clamp circuit allows the oscillator to operate and provides the square wave output. This card is used mainly in timing and pulse forming circuits. In the typical application shown, the oscillator is controlled by a voltage mode trigger and drives into the sample pulse driver.

Circuit Description

Assume the circuit conditions as noted on the schematic. The dash-line circuitry indicates input and output loading.

Oscillator Off. With a −S input at pin A, transistors T2, T4 and T5 are partially conducting and T1, T3 and T6 are off. The output at pin D is at +0.2v. Current flow from the divider network of R4 and R5 through T2 and R8 to +6v holds the common T1 and T2 emitters at −1.8v and the base of T4 near −7.5v. T3 is reverse-biased off and current through its collector divider network sets the base of T6 at −6.8v. T6 and T5 common emitters attempt to follow the base input of T6 to −7v. However, T5 goes into conduction and clamps the common T5 and T6 emitters at −6.2v and establishes the output at pin D to +0.2v.

With the base of T4 held at −7.5v, a constant current flows through T4 and the 1mh inductor. Little voltage is dropped across the low resistance inductor and T1 base is set near ground potential. T1 is reverse-biased off as conduction through T2 keeps the common emitters of T1 and T2 at −1.8v.

Oscillator On. A positive shift at the clamp input (pin A) reduces the forward bias on T2. Reduced current flow in T2 allows the common emitters of T2 and T1 to become less negative and the common collectors to become more negative. T4 conducts less and the current through the 1mh inductor tries to drop. This change is resisted with a counter-EMF that reflects a positive potential onto T1 base and prevents T1 from going into instant conduction. As soon as the counter-EMF dissipates, T1 does conduct, drawing the common emitters of T1 and T2 negative and the common collectors positive. T4 conducts more current, charging the network capacitors and driving T1 base more negative. T4 continues to conduct harder until the capacitors are charged and a constant current again flows through the inductor. T1 base starts to become less negative, and T4 starts to conduct less. Again counter-EMF drives T1 base positive, and a cycle is complete.

The frequency is determined by the values of inductance, capacitance, and resistance in T4 collector circuit. Charge and discharge time of the LC network are the determining factors. Therefore, the frequency can be changed by adjusting the variable capacitor (C23). Oscillations can continue as long as the common base and common collector of T1 and T2 are not restricted by any conduction in T2.

Square Wave Output. Each time the common emitters of T1 and T2 seek a positive level, T3 becomes forward biased and conducts. T3 collector becomes less negative and T6, an emitter follower, conducts. As soon as T6 emitter (common with T5 emitter) rises to −6v, T5 cuts off because of emitter-base reverse bias. The output at pin D rises to +6v.

T1 and T2 emitters again go negative as the oscillator cycle progresses. T3 cuts off, T6 cuts off, and T5 returns to partial conduction. Output pin D returns to ground.

The overall circuit operation can be summarized: T4 is the oscillator transistor, with the frequency-determining resonant circuit at its collector. Feedback to T4 base from the resonant circuit is done through T1. This feedback can be cut off, or clamped, by T2. T3 detects the oscillations, which are amplified by T6 and clipped by T5. The output is approximately 6v in amplitude with a frequency of about 13μs.